DFM-aware Detail Routing

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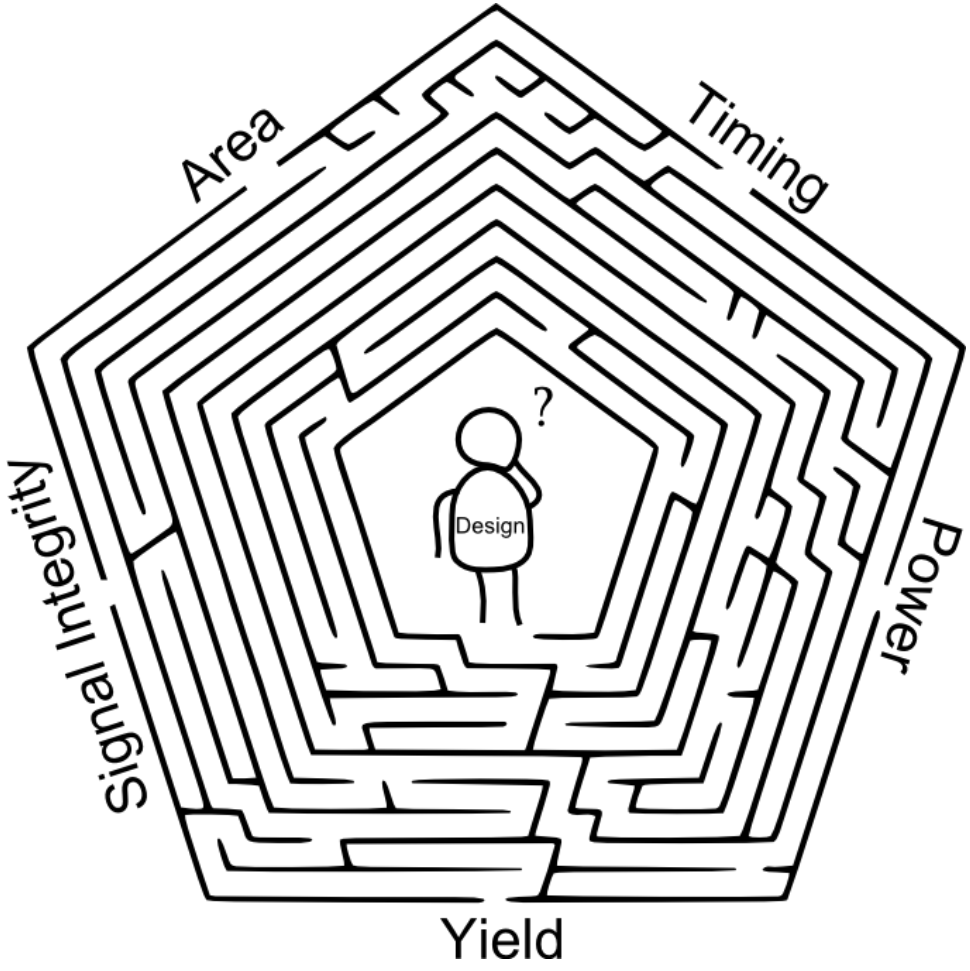
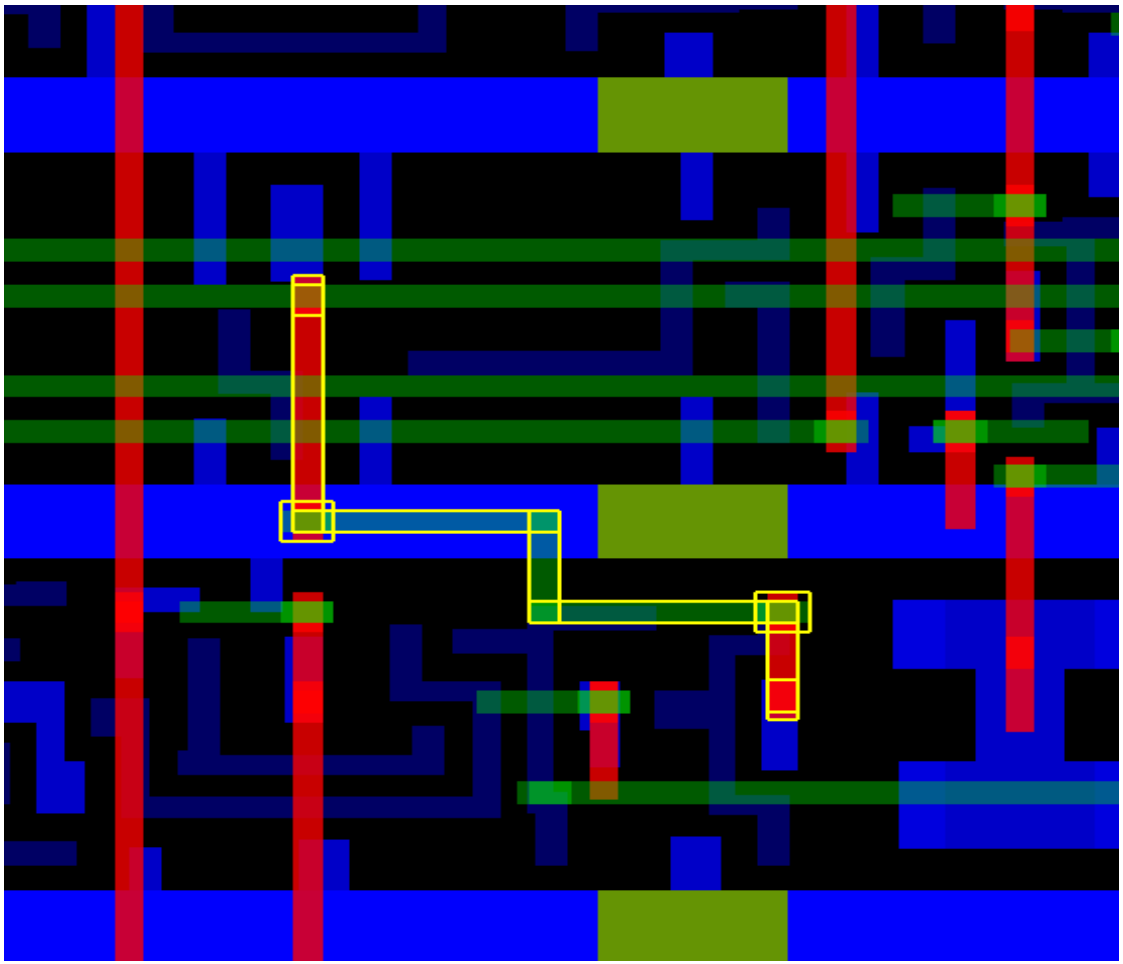


Outline

- Detail routing
- Lithography hot-spots
- DFM
- Rule- and model-based DFY criteria estimation
- Integration into routing flow
- Algorithmic approaches

Detail Routing

Goal is to determine the exact shape of the wires



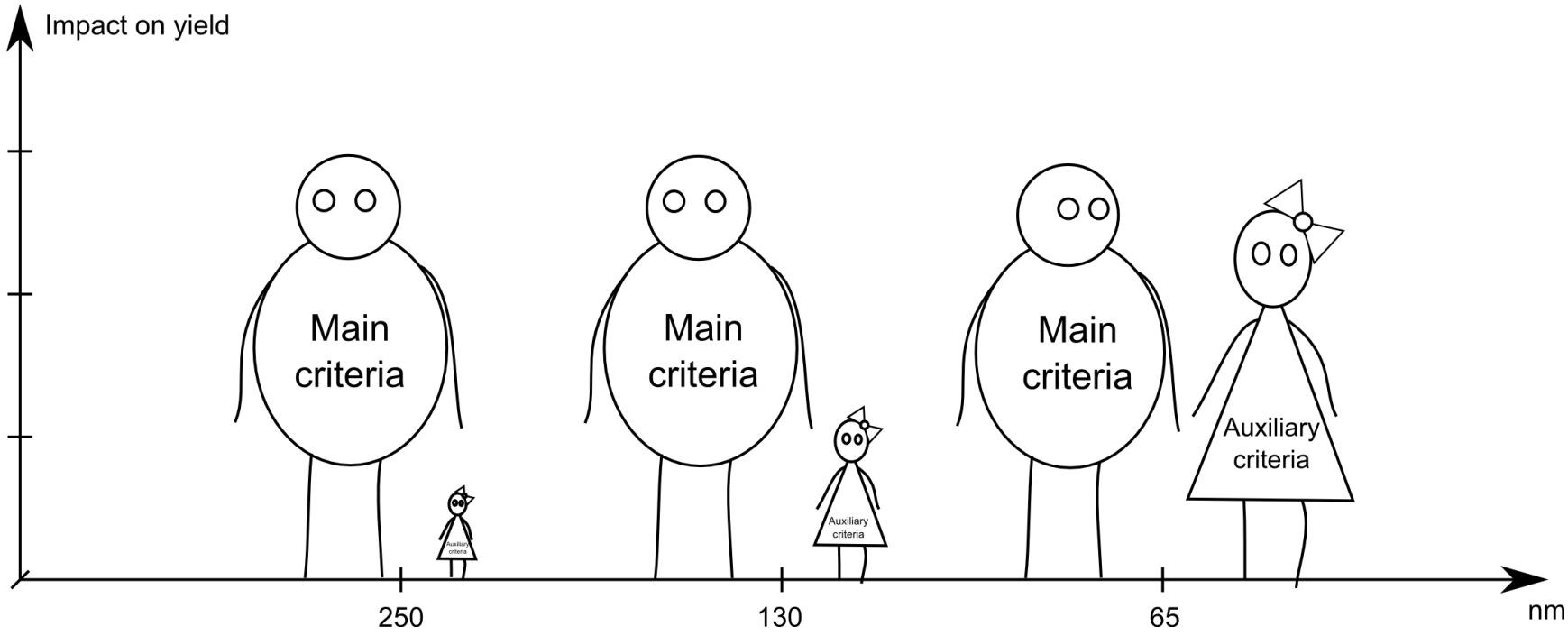
Final Detail Routing Criteria

- Main criteria
  - 100% routability
  - DRC clean design
  - Timing/Power enhancement
- Auxiliary criteria
  - Optical proximity failure minimization
  - Via failure minimization
  - Crosstalk avoidance
  - Planarity enhancement
  - IR-drop minimization
  - EM minimization
  - Minimization of failures due to random defects

Detail Routing Criteria During Run

- Wire length minimization
- Via number minimization
- ???
- All other criteria are post-optimizations
- This is the ad-hoc situation due to gradually introduced effects
- But now…

Increasing Role of “Auxiliary” Criteria



- Role of the auxiliary criteria increases with feature size decrease.
- Below 65 nm neglecting these criteria results in yield so small, that chip production becomes economically inefficient.

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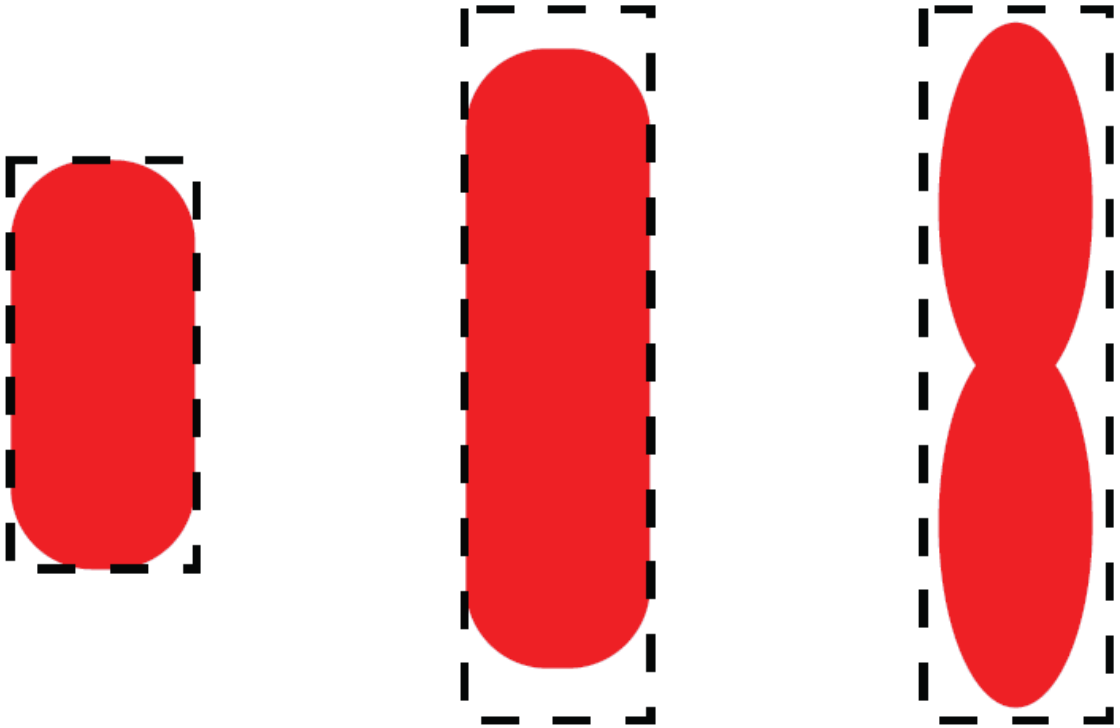
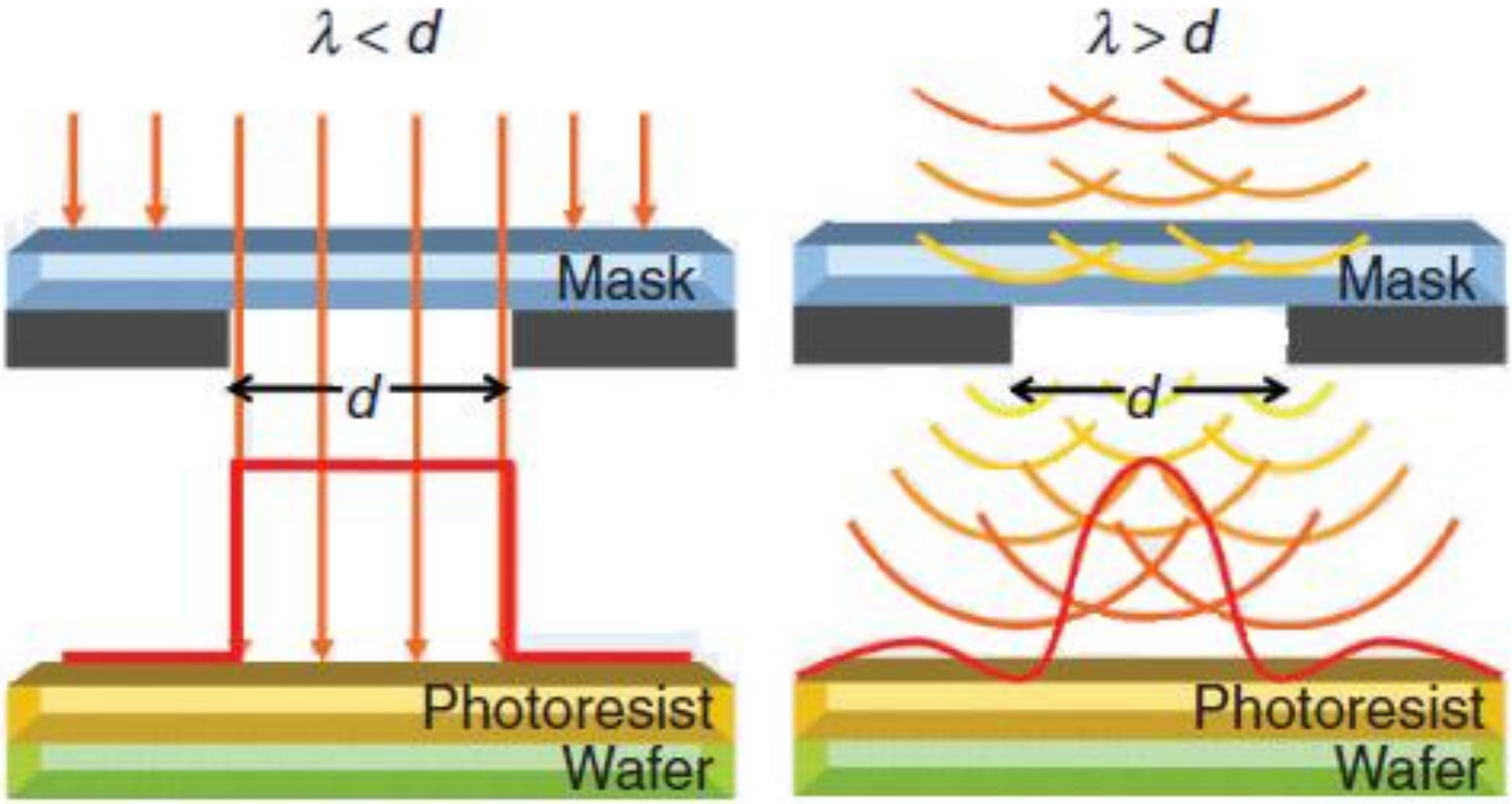
Lithography hot-spots

- Areas prone to defects due to the production issues
- Our goal is to minimize the area of the hot-spots

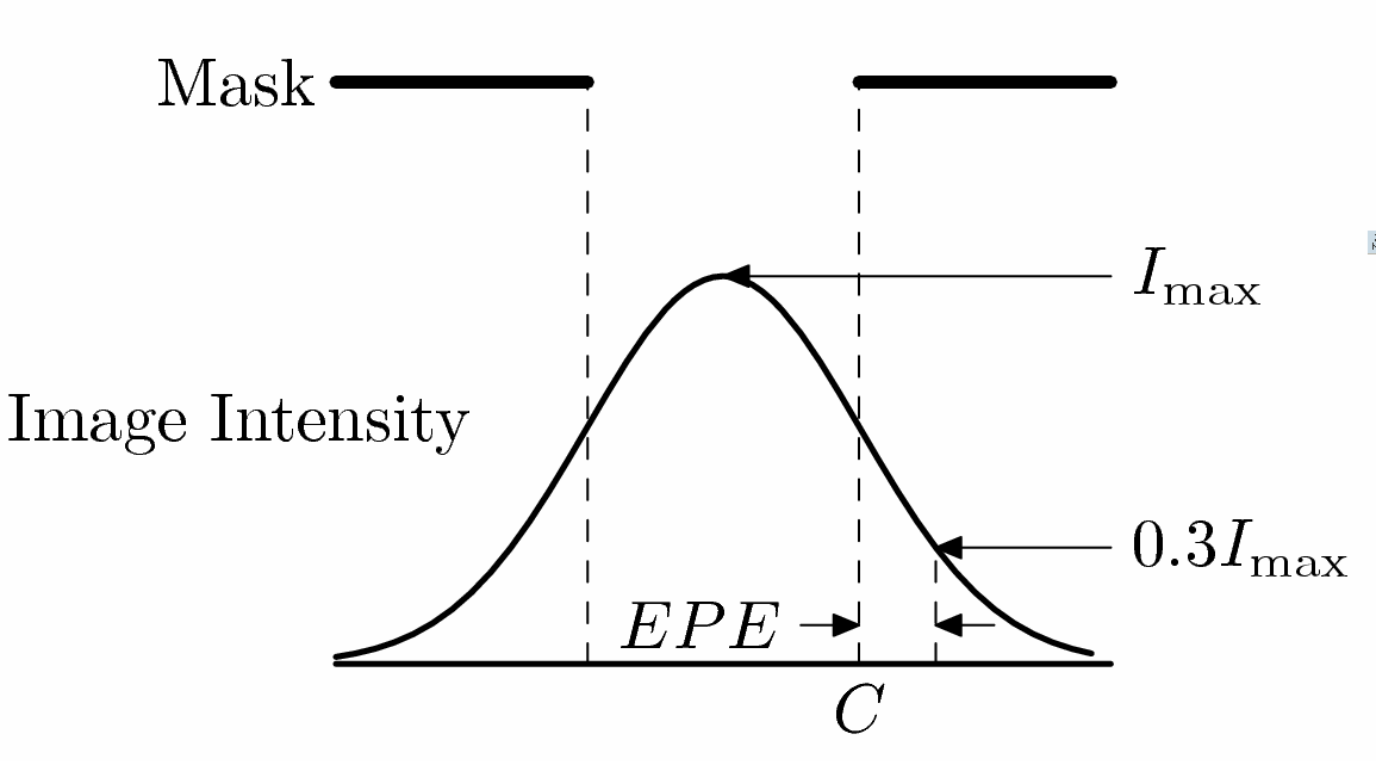


Reason for Lithography hot-spots



- Geometrical optics is no longer valid.
- Simulation is needed to determine actual shapes.

Edge Placement Error Areas as Hot-spots



- Edge placement error (EPE) is a simple estimation.
- EPE guided router can produce correct-by-construct designs.
- Still post-optimization.

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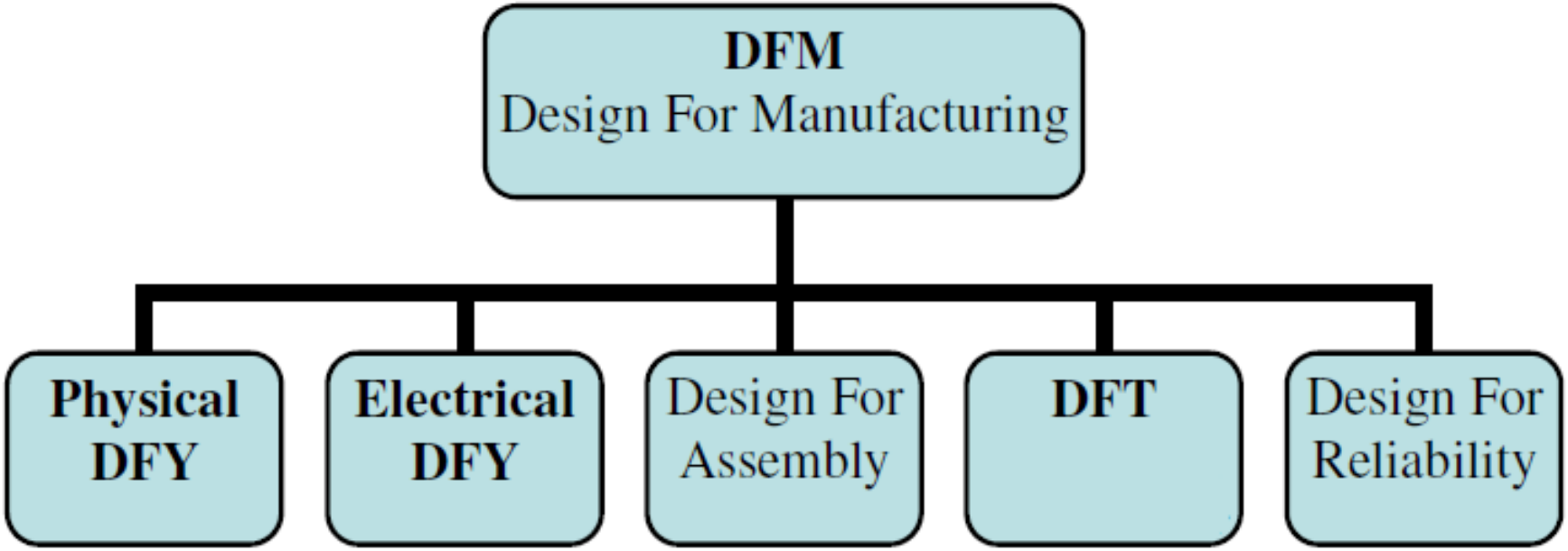
Design for Manufacturability



- The set of measures whose primary focus is to negate production effects.
- DFT – Design for Test.
- We'll talk Physical DFY – Design for Yield.

Design for Yield

- Rule-based
  - Ad-hoc technique
  - Is the result of the gradual feature size reduction
  - Current “mainstream”
  - Uses distance based Design Rule-like recommendations
- Model-based
  - Was shunned for a long time due to its complexity
  - The “source” of rules
  - Provides true estimation of the production effects
  - Models production process with more or less accuracy

Rule-Based DFY

+ Well established
+ Integrated into contemporary EDAs
+ Simple metrics (distance-based)
- Difficult formalization
- Huge amount of rules
- No smooth trade-off between yield and the other parameters (Power, Timing, SI)
- Rules are checked at the late stages

Model-Based DFY

+ Offers a smooth trade-off between yield and the other parameters (Power, Timing, SI)
+ Closer to optimal solution
+ Models can be simpler than rules
+ Used at the synthesis stage, hence little to no post-processing required
- Models can be very sophisticated
- Has no native support in modern EDAs

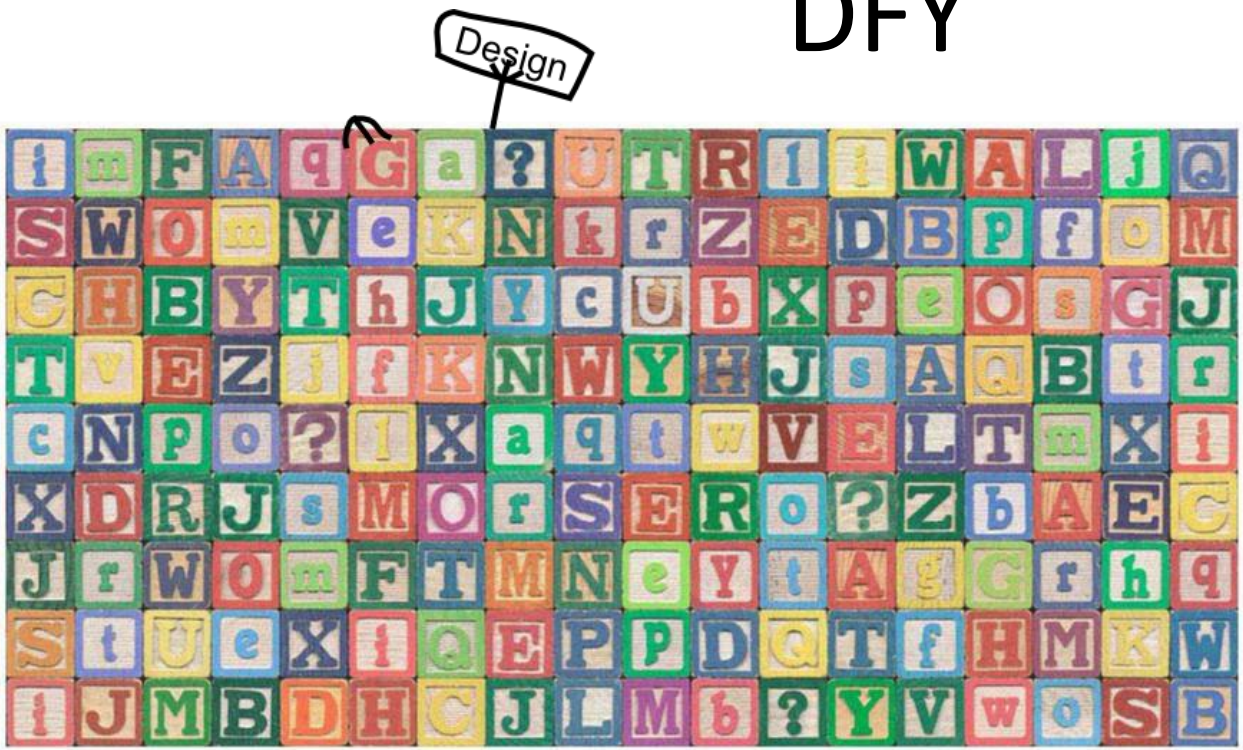
DFY

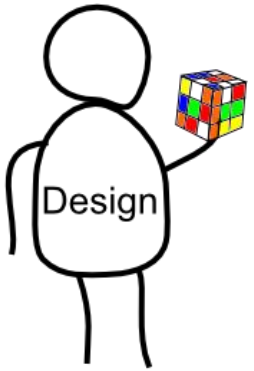
Rule based

Model based

- Design rule is simple, standardized and well known to everyone.
- Model of technological process is very sophisticated and there’s no naive way to solve it.

DFY





- With feature size decrease, number and complexity of rules are increasing, while model changes slightly.
- Also you can always sacrifice accuracy and lower computational complexity, while you can not decrease number of rules.

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How Do Criteria Can Be Estimated?

- Silicon simulation

  Very complicated, but very accurate way. For the modern VLSI this approach is almost unacceptable.

- Simplified models

  These include less accurate models for aerial and litho-image, metal density, variational and systematic edge placement error.

- Distance-based hot-spot reduction

  The simplest method, very similar to rules. It overestimates hot-spot area, but is very fast.

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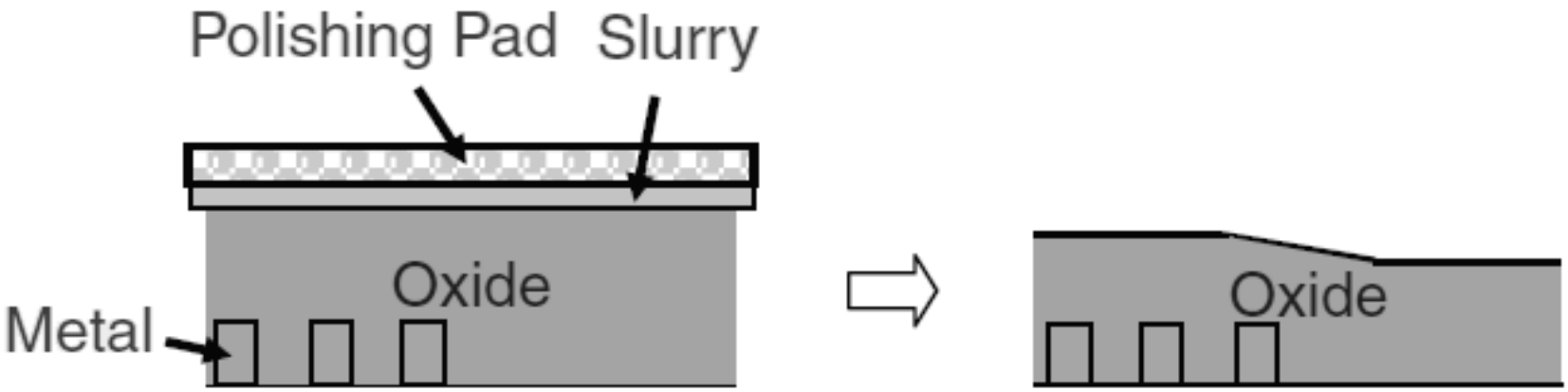
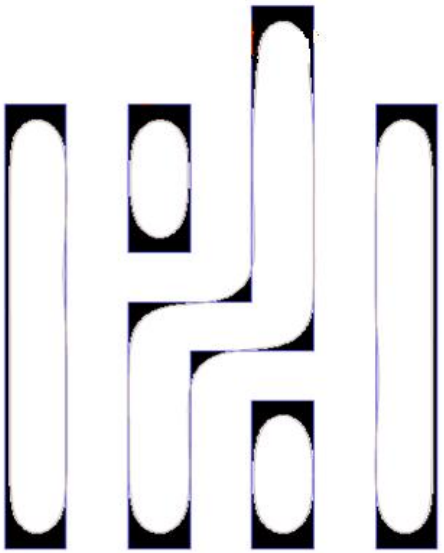


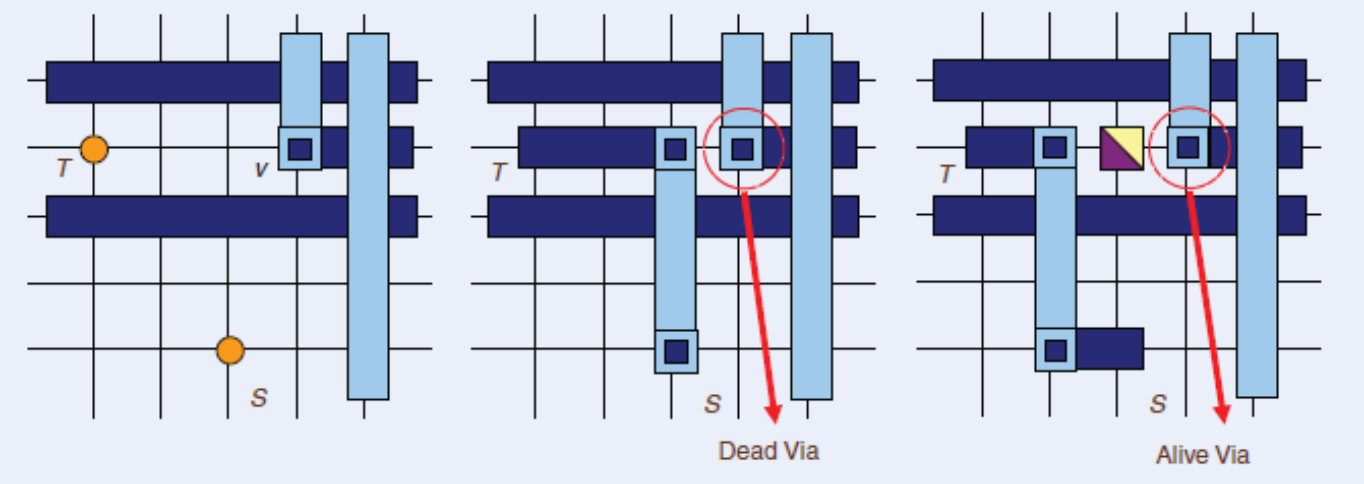
Design-specific thickness variation.



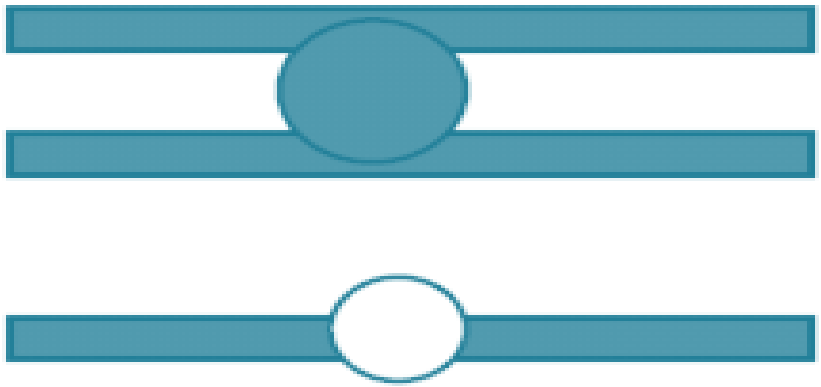
Jogs introduce additional hot-spots.

Implementation

- CMP awareness/Density uniformity
  - Wire spreading improves planarity, since the polishing process becomes more isotropic.
  - Dummy fill is the necessary modern technique to improve planarity, so it must be taken into account.
- Jog minimization
  - Wire straightening (L-shaped wires) reduces lithography errors, since simpler forms tends to be less distorted.



Via-redundancy aware routing



Short and open defects due to random defects

Implementation

- Via failure
  - Via redundancy serves as “back-up system” for failed vias. Although for deeper submicron redundant vias increase wire capacitance and introduce noise and signal reflection.
  - Via metal enclosure serves as a guard from layer misalignment.
  - Overall via number minimization is of course a good thing to do.
- Random defects
  - Wire spreading lowers probability of short between neighboring wires.
  - Wire reordering can reduce critical area of short, interleaving long and short wires.
  - Wire width/spacing regulation lowers both probability of short and open.

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Approaches – Maze Routing

Increase paths' cost for:

- Proximity to each other – for lithography improvement, wire density annealing and decreasing random defects.
- Via proximity – for lithography improvements and increasing abilities to place redundant vias and metal enclosure.
- Bends – for improve lithography image.

Approaches - Heuristics

- Maximize density uniformity – for improving planarity.
- Prefer L- and I-shapes to Z-shapes – for improving lithography image.
- Mix long/short segments – for decrease random defect influence.

Approaches – Other

- Rip-up and reroute
  - Introduce new obstacles in lithography “hot-spots”, provides wide range of area-minimization based improvements.
- ILP/NLP
  - Find optimal solution for wire width/spacing and segment order to minimize “hot-spot” and random defect sensitive area.

Conclusions

- Detail routing stage can optimize yield.
- Doing this as a post-optimization reduces flexibility and quality of solution.
- Current methods should be adapted.
- While adapting the existing methods is possible, the better solution is to seek for a new methods.
- Goal is to synthesize maximizing yield routing pattern during one iteration.