Unified Logical Effort [1]

Hela Jedda

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[1] “Unified Logical Effort- A Method for Delay Evaluation and Minimization in Logic Paths with RC Interconnect“ by Arkady Morgenshtein, Eby G Friedman, Ran Cinosar and Avinoam Kolodny

Speed is important

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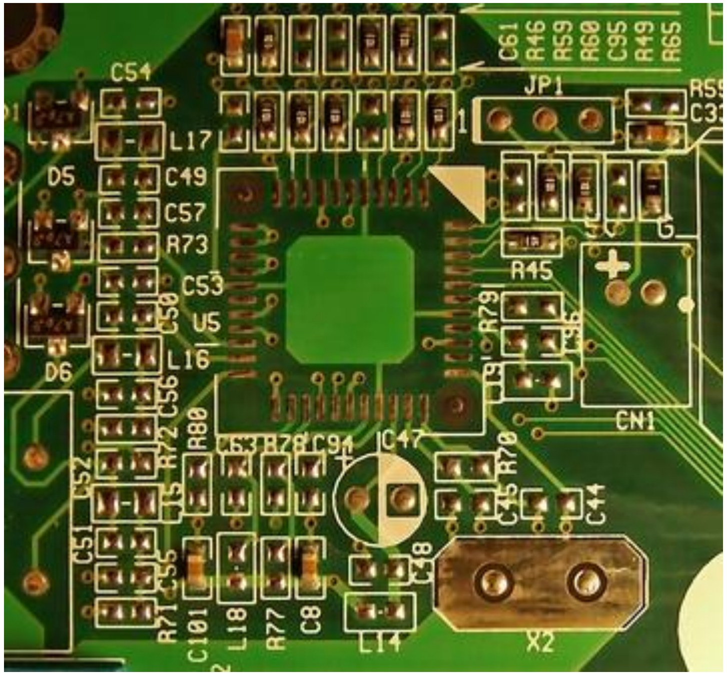
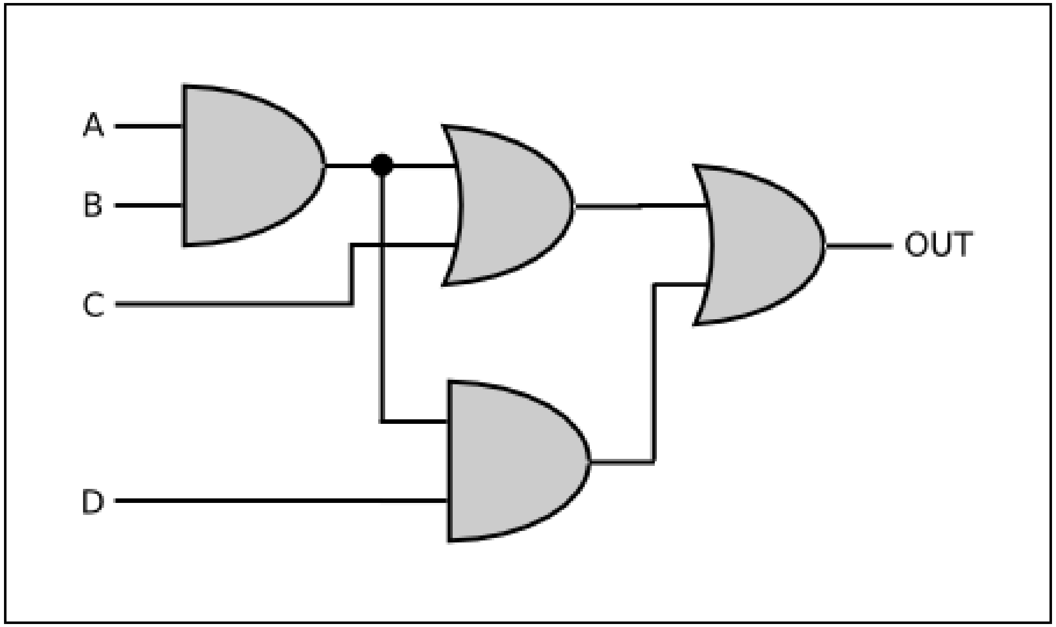




We need fast gates!!

Fast gates

- How to make the gates fast?
- How to have the least delay?

Idea?

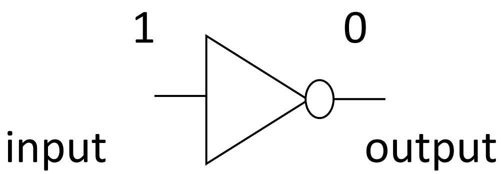
1. To find a mathematical expression of the delay
2. To derivate it
3. Derivative schould be equal to 0

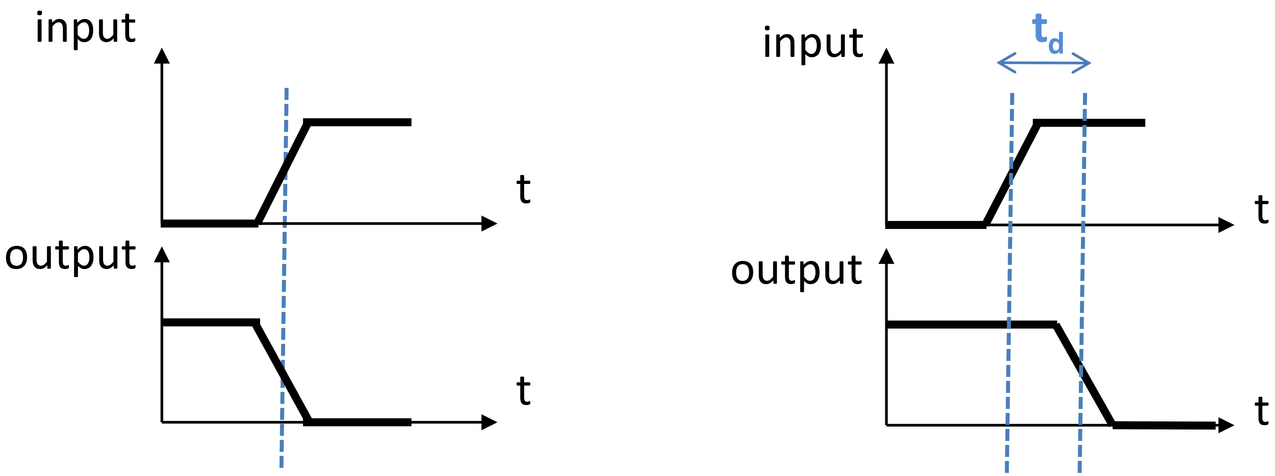
Unified Logical Effort

Outline

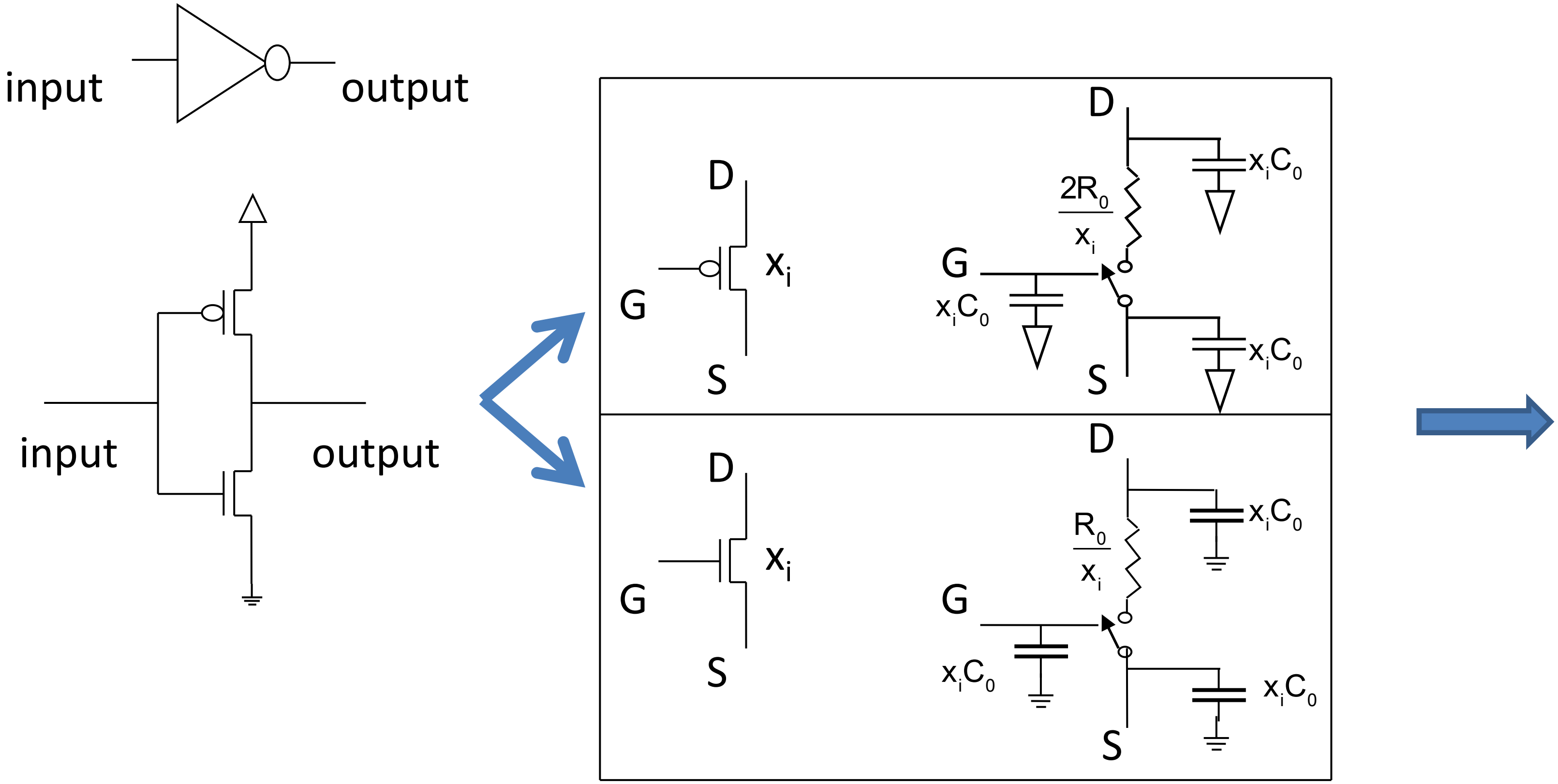
- Introduction about the gates
- Delay´s components
- Delay of gates without interconnect
- Delay of gates with interconnect
- Minimizing the delay with Unified logical Effort
- Conclusion

Introduction about the gates

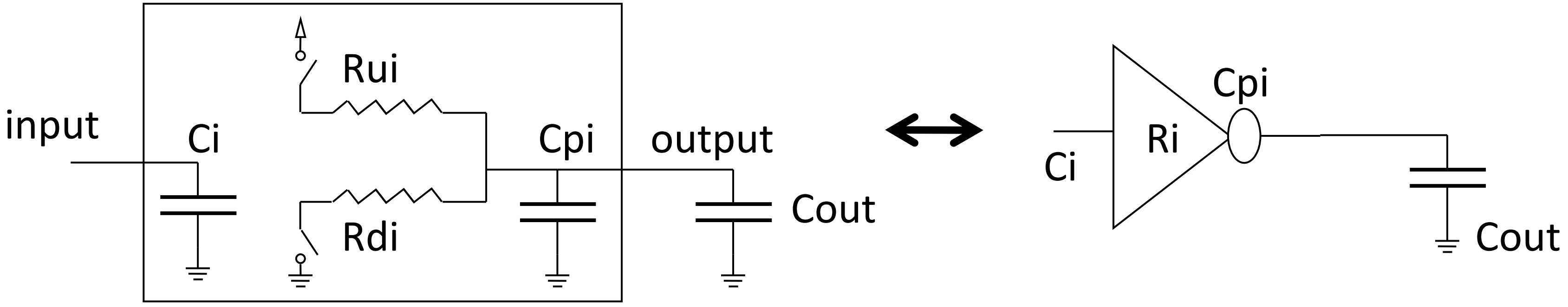




Introduction about the gates



Introduction about the gates



General RC Inverter Model

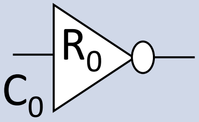
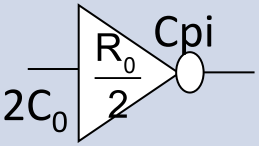
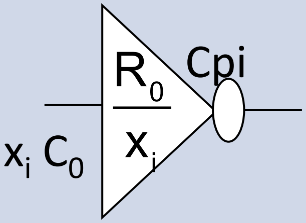
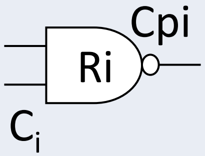
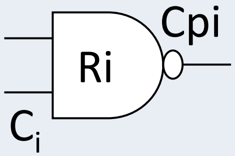
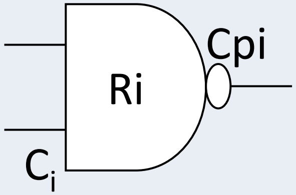
Rdi : pulldown resistance

Rui : pullup resistance

Cpi: parasitic cap of gate from drain capacitances

Introduction about the gates

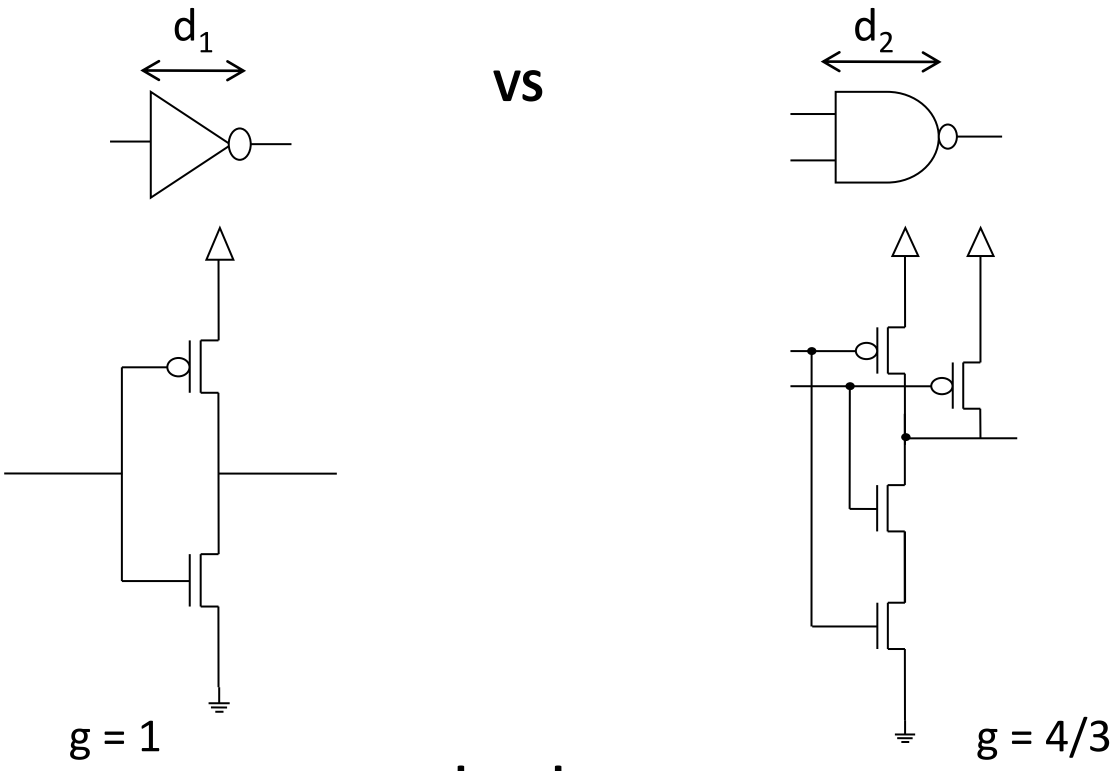
The minimum sized inverter

Width	1	2	x_i
Inverter			
NAND			

$$C_i \propto C_0 x_i$$

$$R_i = \frac{R_0}{x_i}$$

Delay´s components



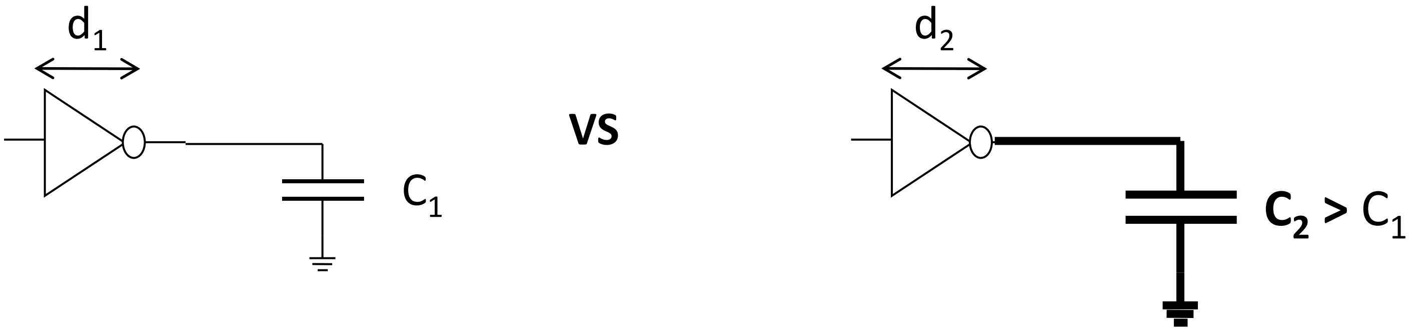
$d_1 < d_2$

The delay depends on the **topology of the gate**.

Logical Effort

	Number of inputs			
Gate type	1	2	3	n
inverter	1			
NAND		4/3	5/3	(n+2)/3
NOR		5/3	7/3	(2n+1)/3

Delay´s components



$$\mathbf{d_1 < d_2}$$

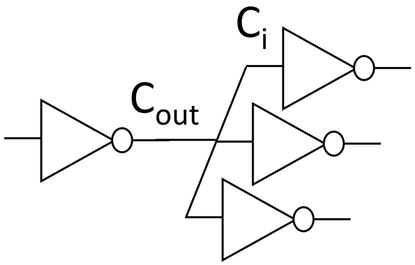
The delay depends on the **output capacitance**.

$$h = \frac{C_{out}}{C_i}$$

Electrical Effort

$h = C_{out}/C_i$

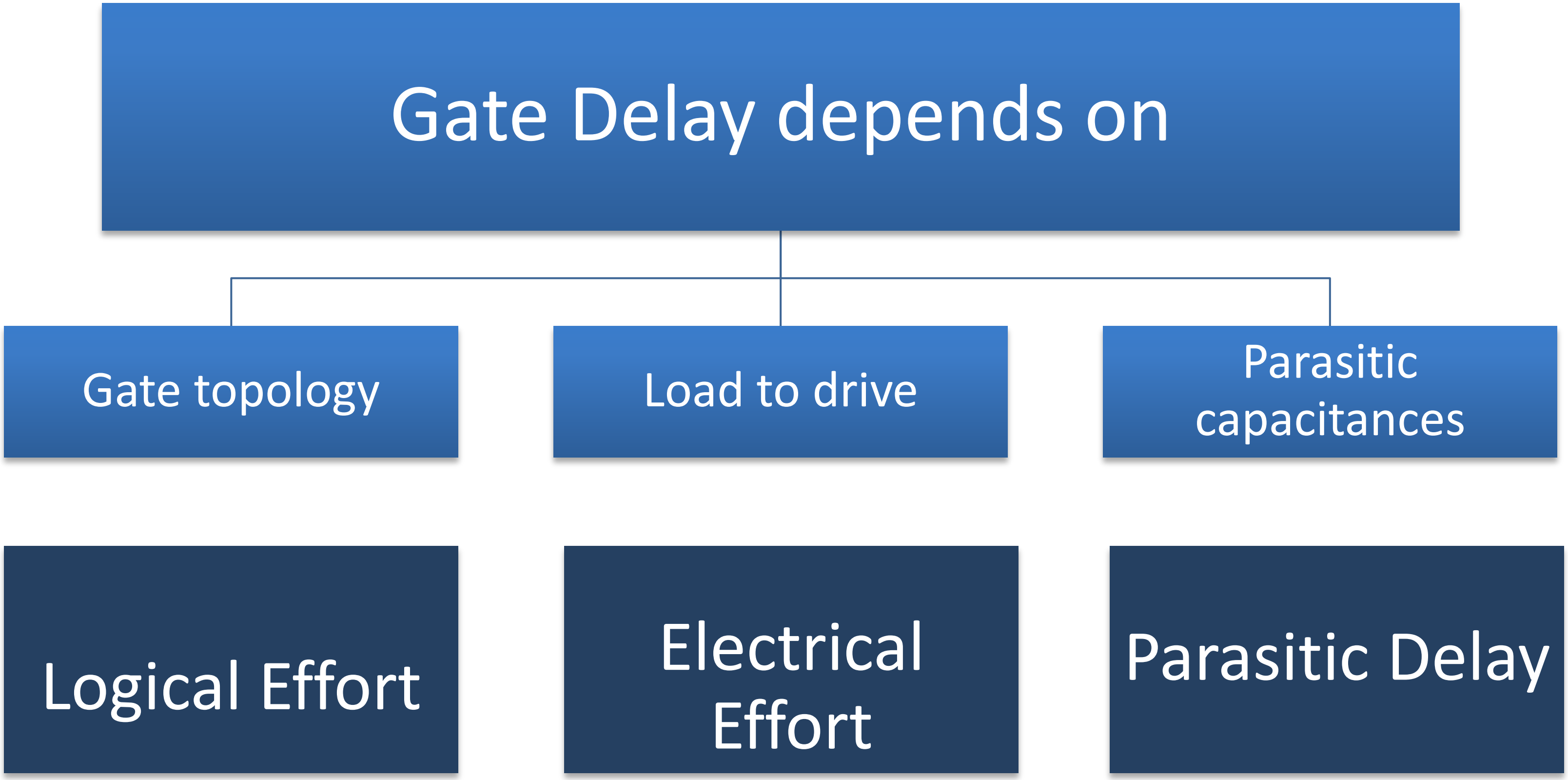
e.g.



$h = C_{out}/C_i \;\; = 3$

Parasitic delay

Gate type	Parasitic delay
inverter	p_{inv}
n-input NAND	np_{inv}
n-input NOR	np_{inv}



Gate Delay depends on

Gate topology

Load to drive

Parasitic capacitances

Logical Effort

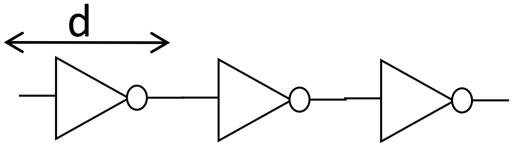
Electrical Effort

Parasitic Delay

$$d = g \quad . \quad h \quad + \quad p$$

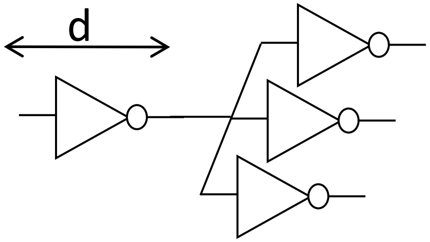
Examples

1.



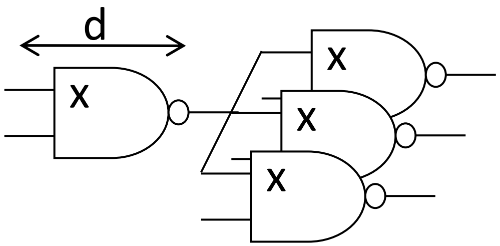
$$\left.\begin{aligned} g_{inv} &= 1 \\ h = \frac{C_{out}}{C_i} &= 1 \\ p_{inv} &= 1 \end{aligned}\right\} \Rightarrow \begin{aligned} d &= g * h + p \\ &= 1 * 1 + 1 = 2 \end{aligned}$$

2.



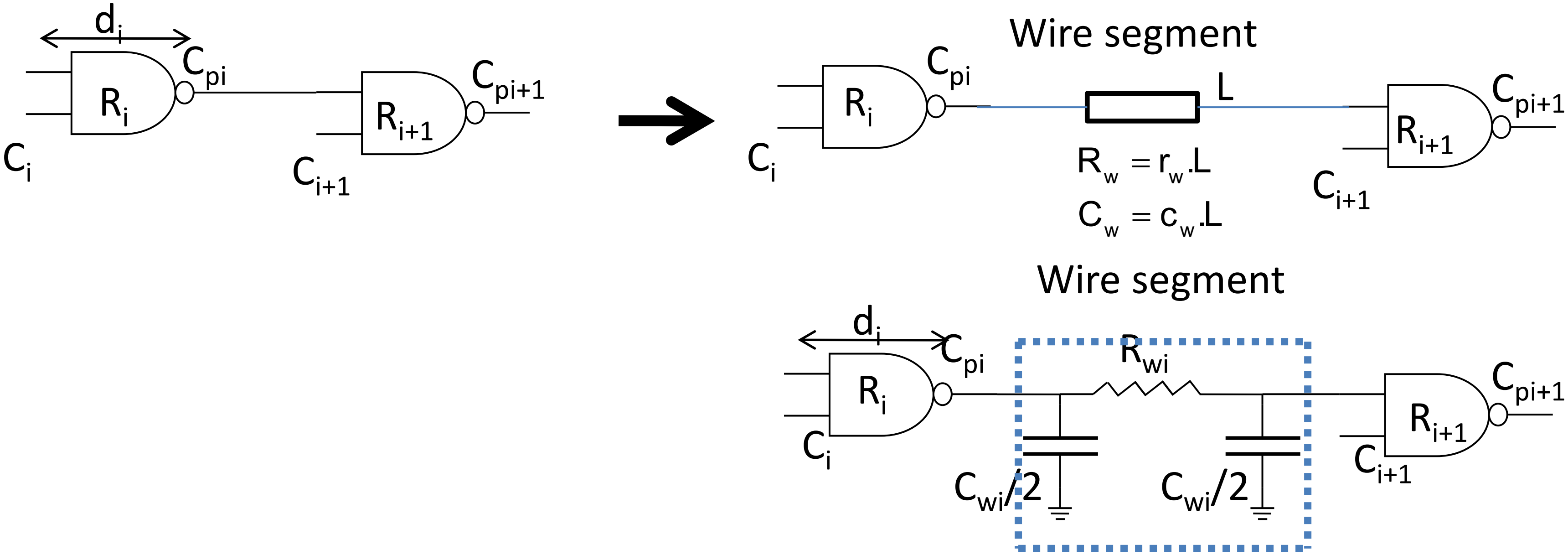
$$\left.\begin{aligned} g_{inv} &= 1 \\ h = \frac{C_{out}}{C_i} &= 3 \\ p_{inv} &= 1 \end{aligned}\right\} \Rightarrow \begin{aligned} d &= g * h + p \\ &= 1 * 3 + 1 = 4 \end{aligned}$$

3.



$$\left.\begin{aligned} g_{NAND2} &= \frac{4}{3} \\ h = \frac{C_{out}}{C_i} &= 3 \\ p_{NAND} &= 2 \end{aligned}\right\} \Rightarrow \begin{aligned} d &= g * h + p \\ &= \frac{4}{3} * 3 + 2 = 6 \end{aligned}$$

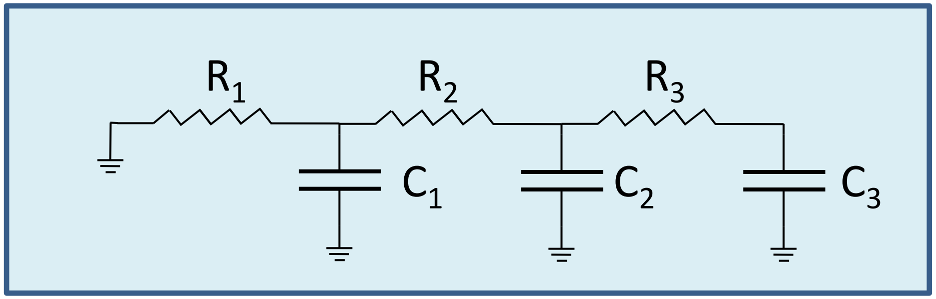
Gates with interconnect



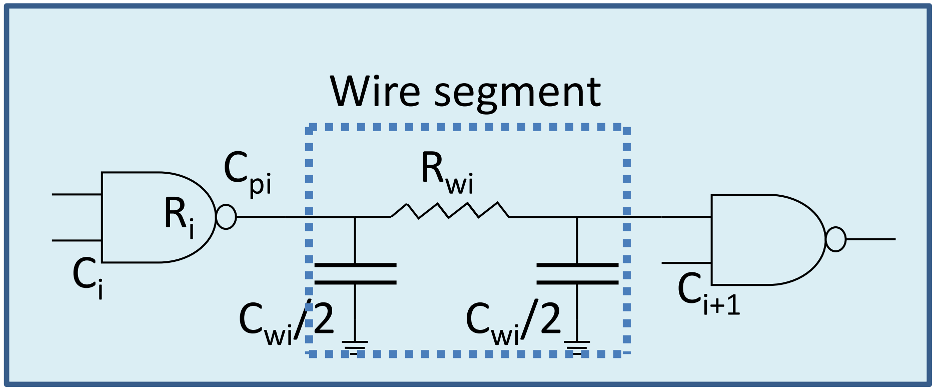
$$d_i = g_i * h_i + p_i$$

$$d_i = ?$$

Elmore Delay



$$D = R_1 (C_1 + C_2 + C_3) + R_2 (C_2 + C_3) + R_3 C_3$$



$$\mathbf{D_i = R_i (C_{pi} + C_{wi} + C_{i+1}) + R_{wi} (0{,}5\, C_{wi} + C_{i+1})}$$

Delay of gates with interconnect

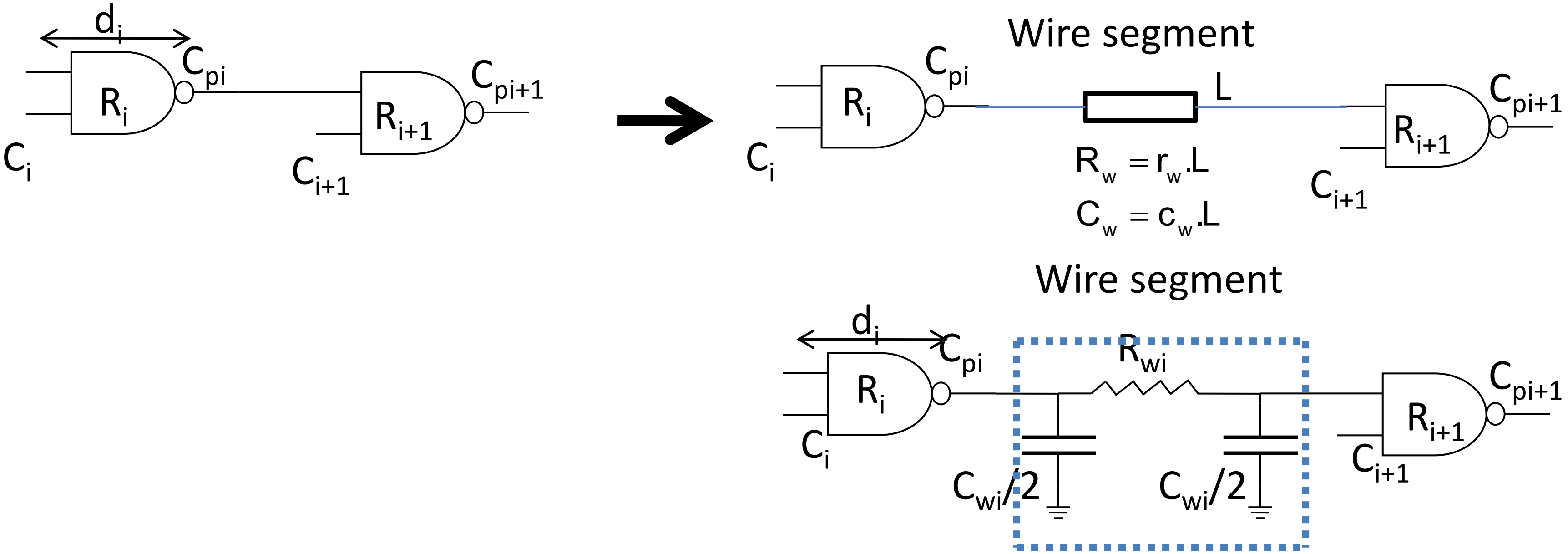
$$\boxed{D_i = R_i\,(C_{pi} + C_{wi} + C_{i+1}\,) + R_{wi}\;(0{,}5\;C_{wi} + C_{i+1}\,)}$$

$D_i = \tau \,.\, d_i$ **with** $\tau = R_0\, C_0$

$$d_i = \frac{R_i}{R_0}\,.\,\frac{C_{wi} + C_{i+1} + C_{pi}}{C_0} + \frac{R_{wi}}{R_0 C_0}\,.\;\; 0{,}5.C_{wi} + C_{i+1}$$

$$= g_i.\;\; h_i + h_{wi} \;\;+\;\; p_i + p_{wi}$$

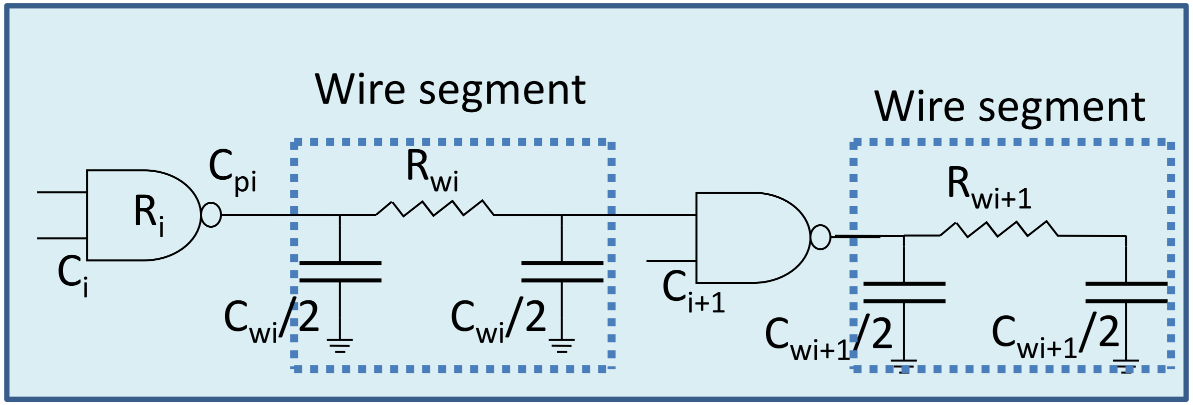
Gates with interconnect



$$d_i = g_i * h_i + p_i$$

$$d_i = g_i * \; h_i + h_{w_i} \; + \; p_i + p_{w_i}$$

Delay Minimization Using Unified Logical Effort

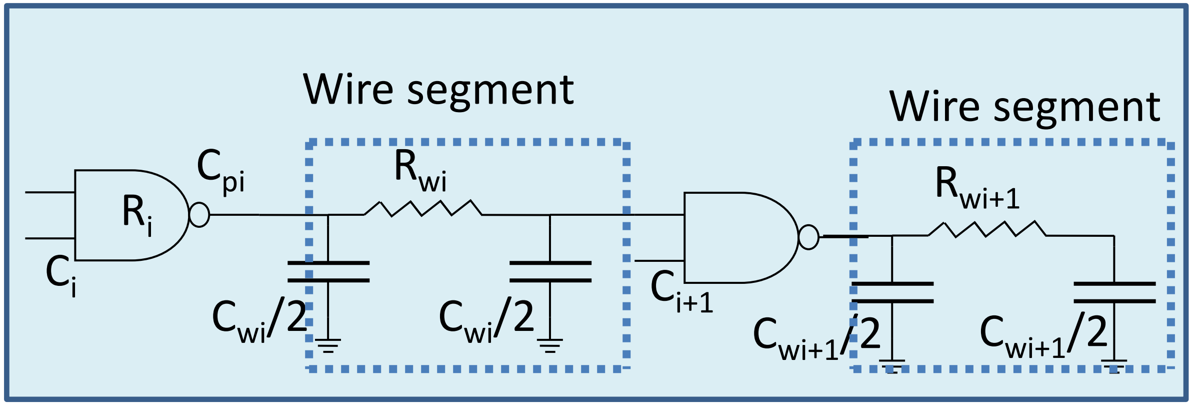


$$d = g_i.\ \ h_i + h_{w_i} \ \ + \ \ p_i + p_{w_i} \ \ + g_{i+1}.\ \ h_{i+1} + h_{w_{i+1}} \ \ + \ \ p_{i+1} + p_{w_{i+1}}$$

Minimization :

$$\frac{\partial d}{\partial h_i} \square\ 0 \qquad \Leftrightarrow \qquad \boxed{\left(g_i + \frac{R_{w_i}.C_i}{R_{0.}C_0}\right).h_i = g_{i+1}.\ \ h_{i+1} + h_{w_{i+1}}}$$

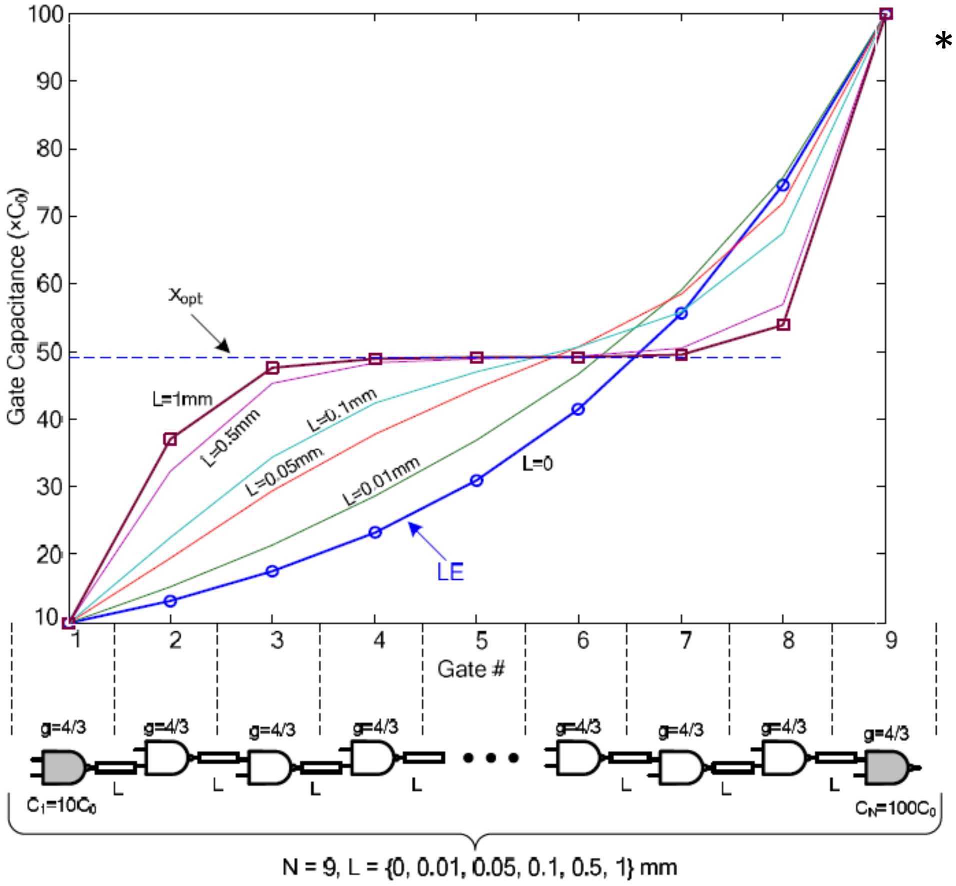
How can we realize this condition?



$$\left(g_i + \frac{R_{w_i}.C_i}{R_{0.}C_0}\right).h_i = g_{i+1}.\ h_{i+1} + h_{w_{i+1}} \quad \Leftrightarrow \quad R_i + R_{w_i}\ .C_{i+1} = R_{i+1}.\ C_{i+2} + C_{w_{i+1}}$$

$$R_i = \frac{R_0}{x_i}, \quad C_i = C_0.g_i.x_i \qquad \Rightarrow \quad x_{i_{opt}} = \sqrt{\frac{R_0}{R_{i-1} + R_{w_{i-1}}} . \frac{C_{i+1} + C_{w_i}}{C_0.g_i}}$$

Examples: die wires have the same length



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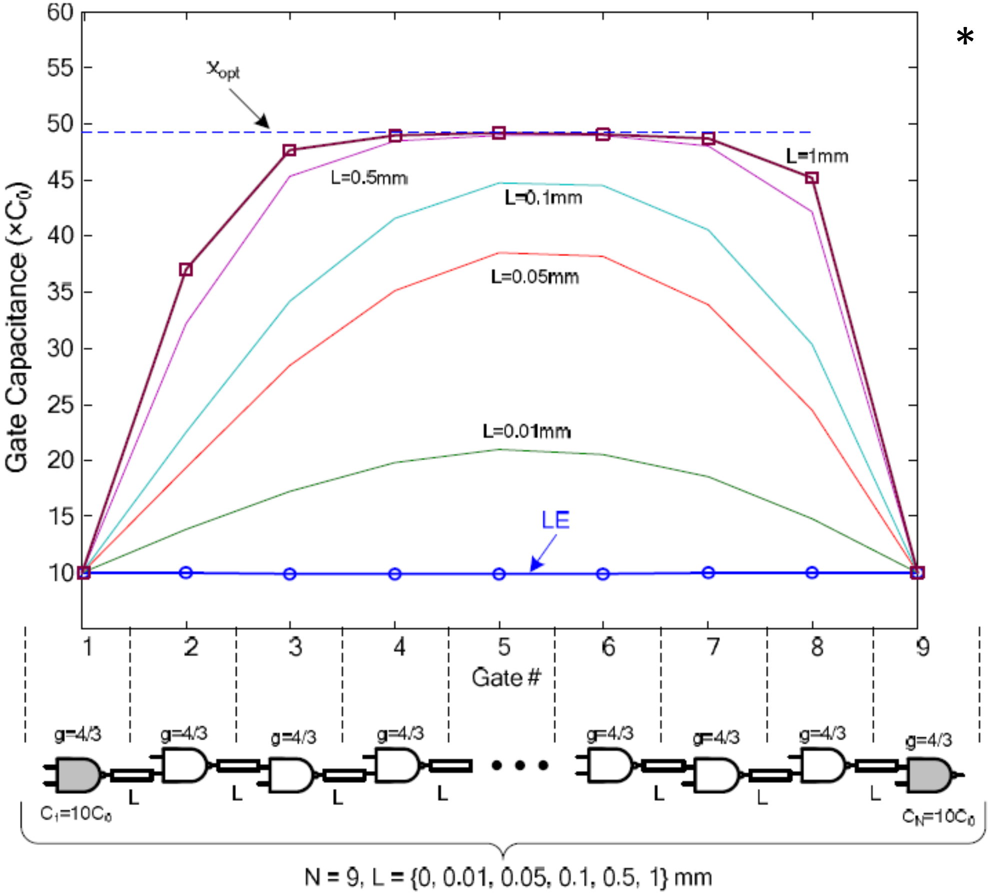
Examples: die wires have the same length



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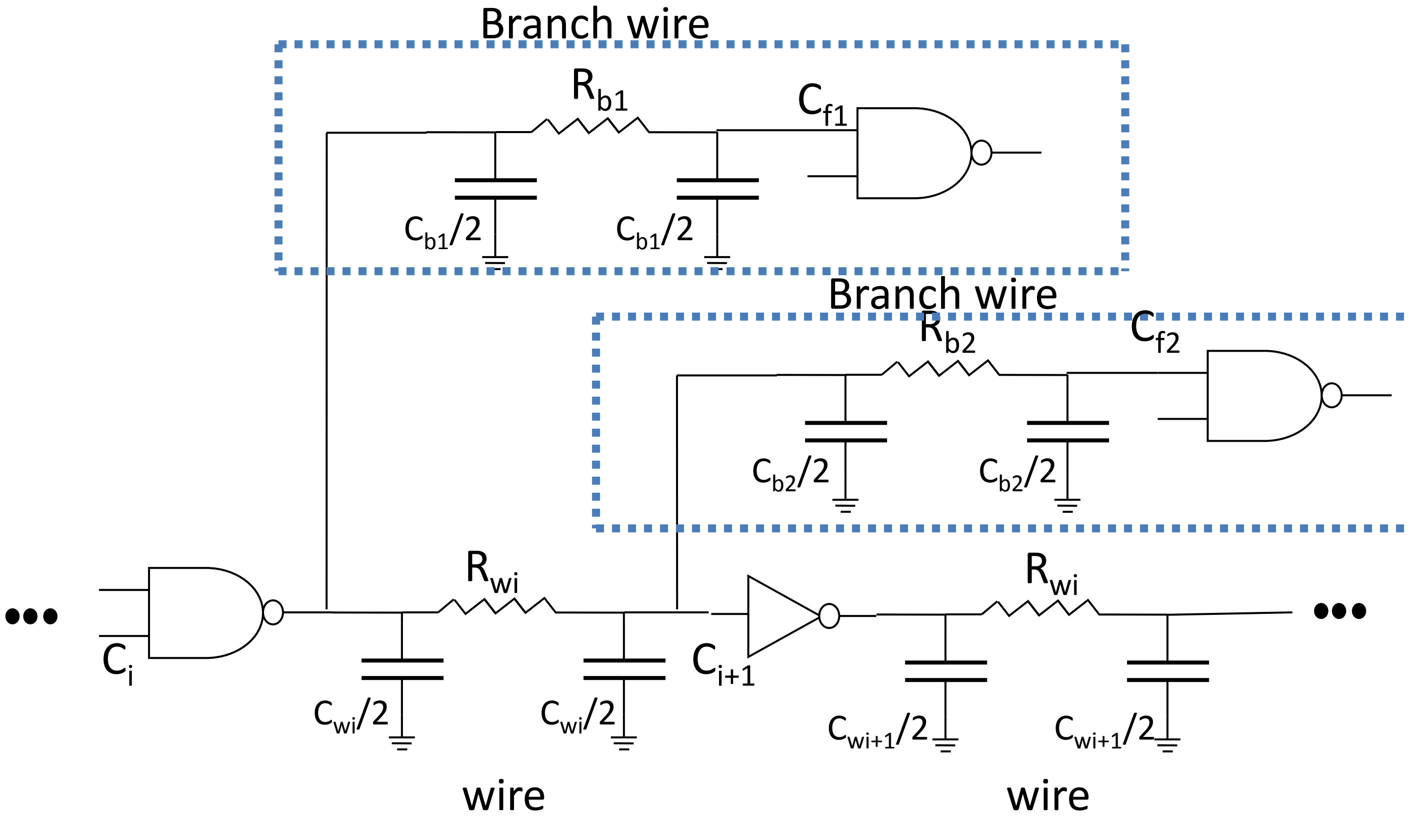
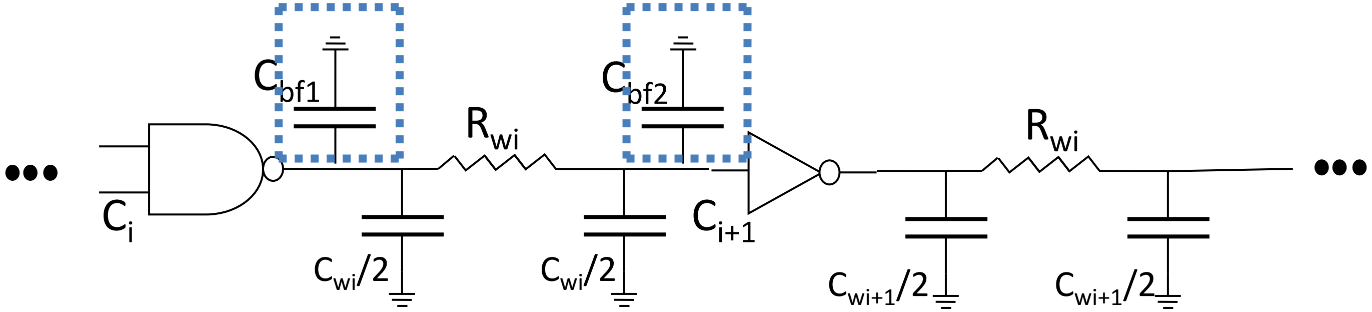
ULE Optimization In Paths With Branches



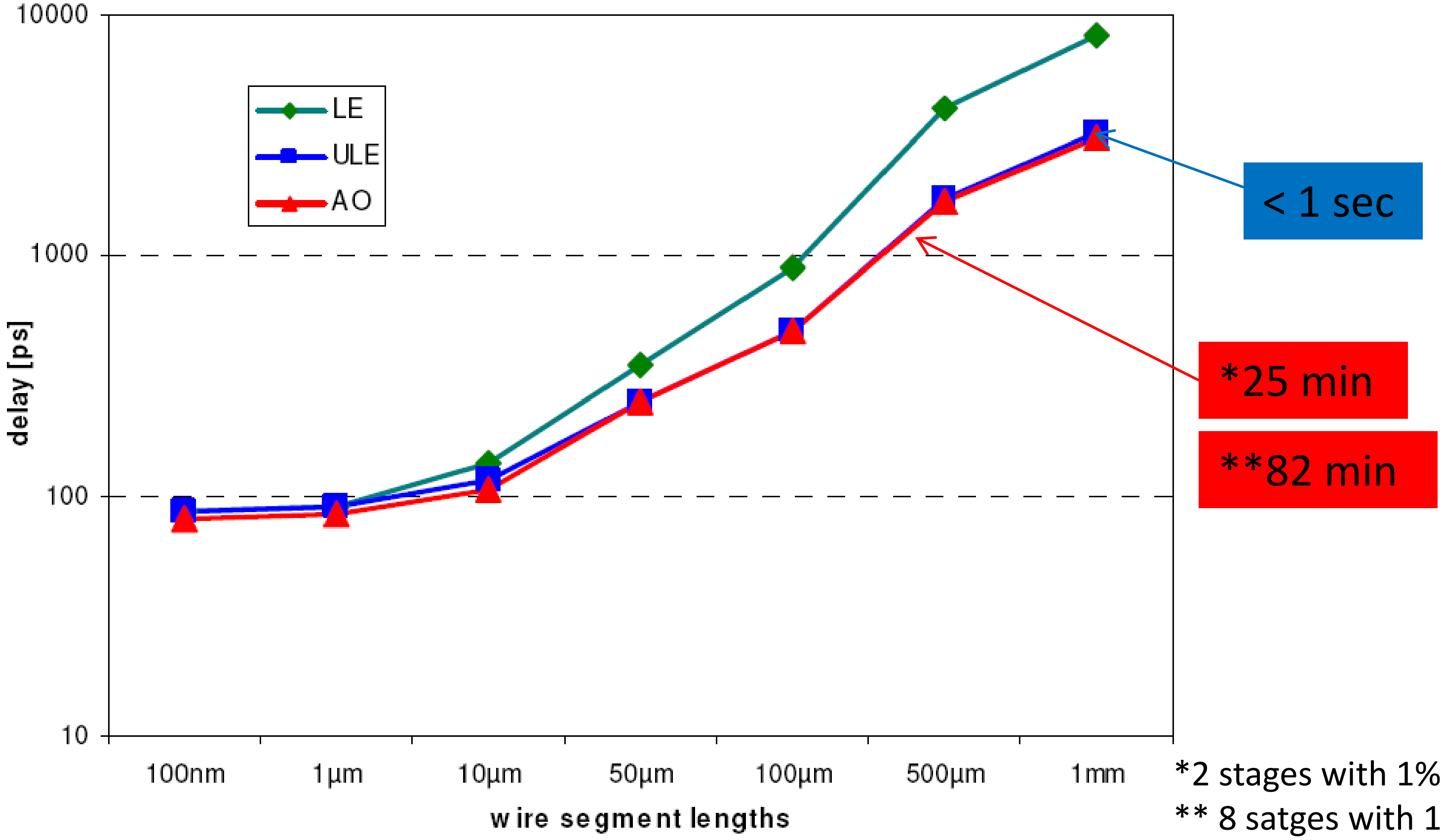
ULE Optimization In Paths With Branches



$$R_i + R_{w_i} \;.C_{i+1} = R_{i+1}. \; C_{i+2} + C_{w_{i+1}} + C_{BF_i}$$

$$\text{mit} \quad C_{BF_i} = \sum_i C_{bf_i}$$

Delay of a carry-lookahead adder for various segment lengths after gate size optimization by LE, ULE and Analog Optimizer (AO)



*2 stages with 1% precision
** 8 satges with 1%precison

Conclusion

- The method of Logical Effort (LE) is limited in presence of interconnect.
- The method of **Unified Logical Effort** (**ULE**) is
  - very simple
  - fast (<1 sec)

  for delay evaluation and optimization of logic paths with general gates and RC wires