MB-JASS

# Asynchronous circuits as alternative way of digital computing

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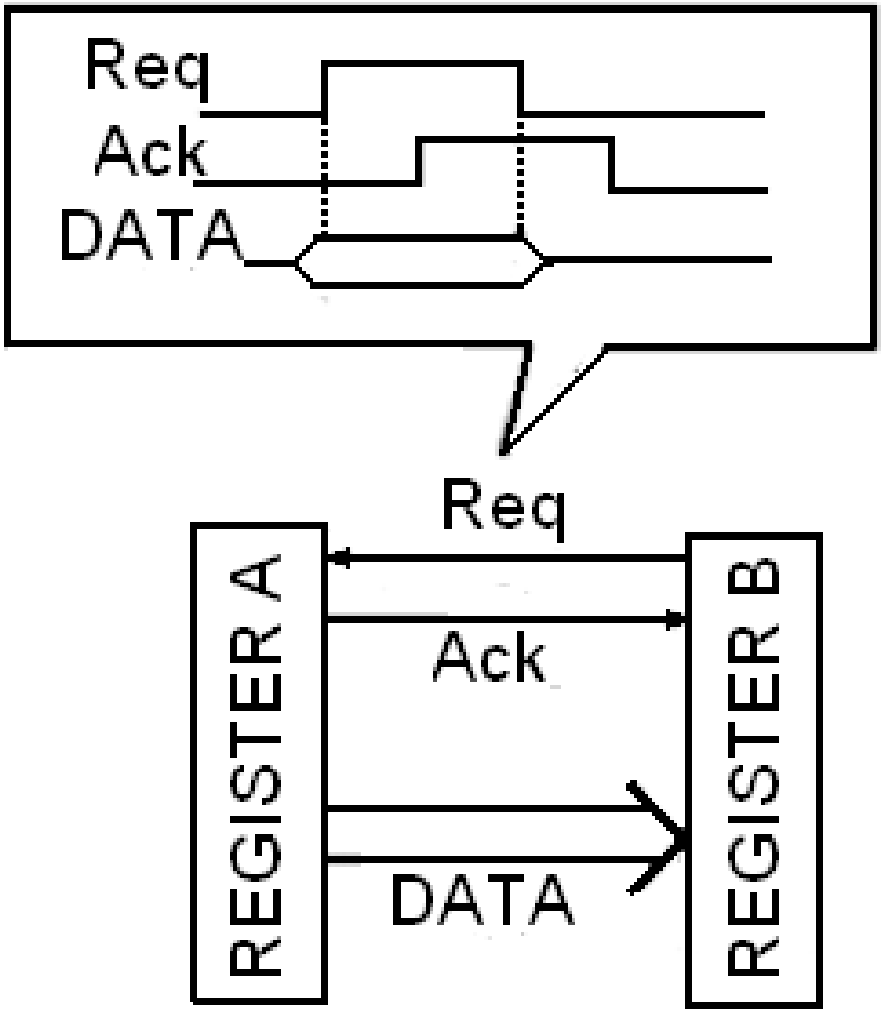
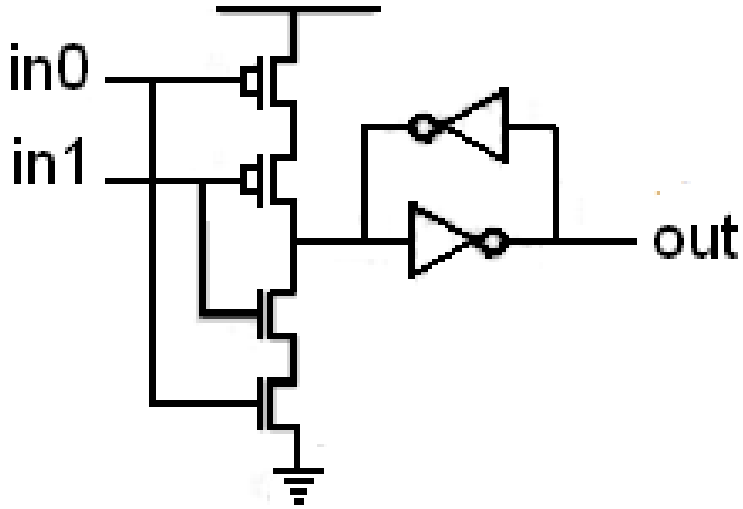
# Synchronous design challenges

- Problem of clock distribution over the crystal.
  - synchronization takes up to 30 % of the crystal area.
  - and power consumption.
- Artificial restriction of performance.
  - global worst-case latency.
- Power consumption.
  - each trigger switches during the clock, even if no new data.
- Emission of electro-magnetic noise.
  - due to simultaneously switching of all triggers over the circuit.

# Principle of asynchronous design

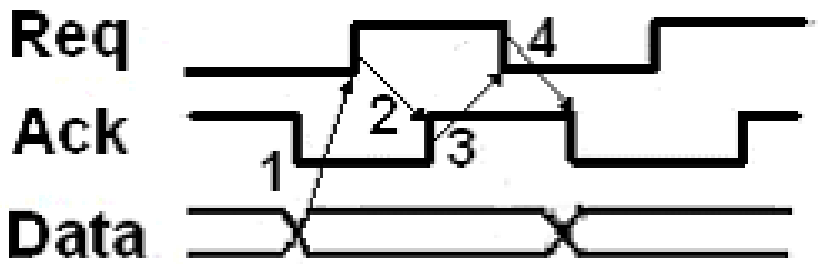


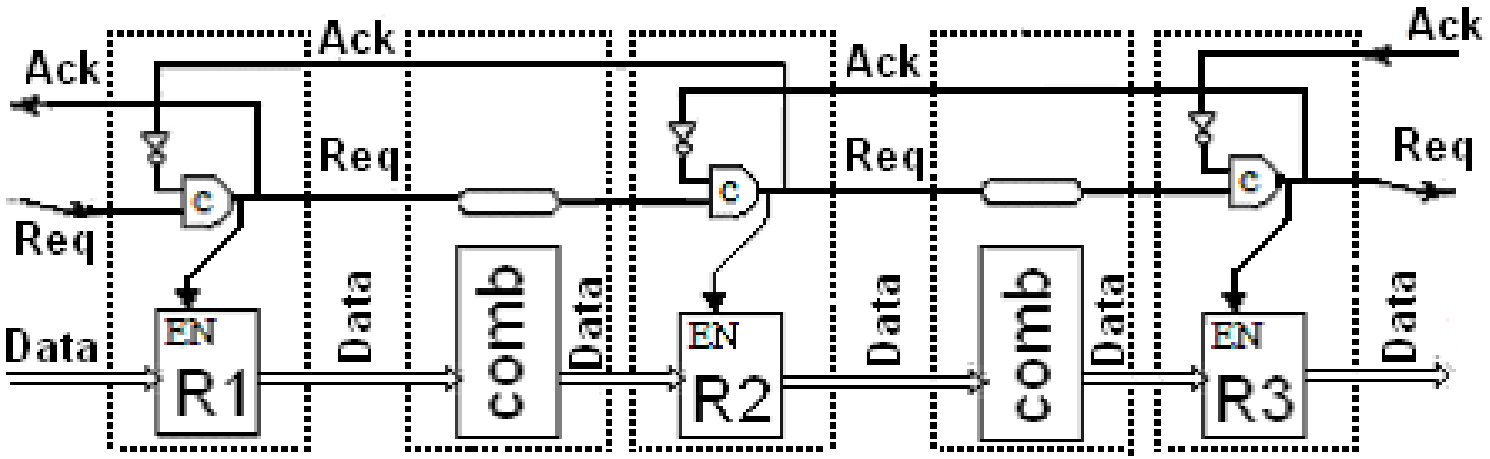
# C-element



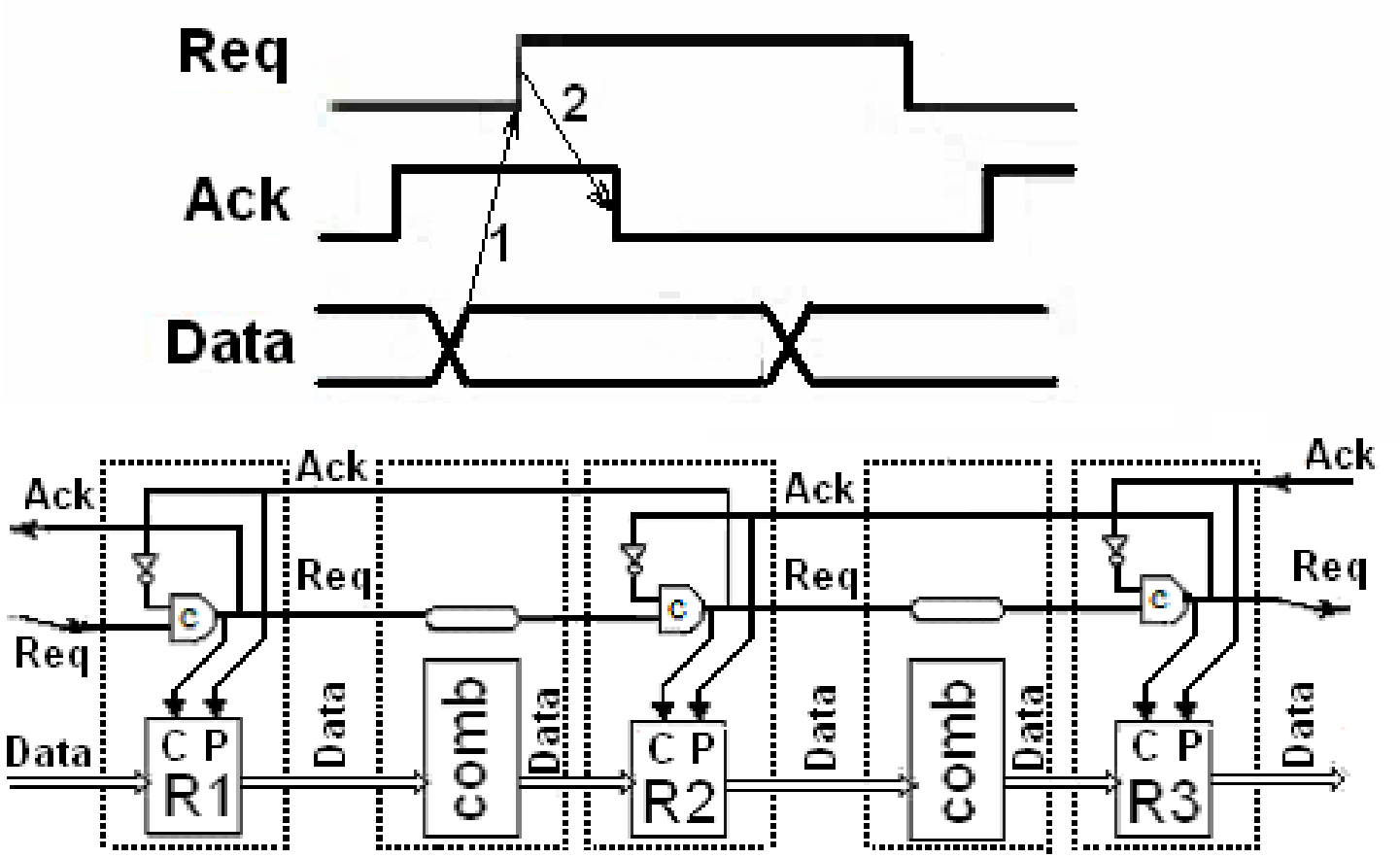

| a | b | y (n) |
|---|---|---|
| *0* | *0* | *0* |
| *0* | *1* | y (n-1) |
| *1* | *0* | y (n-1) |
| *1* | *1* | *1* |

# 4-phase bundled data protocol



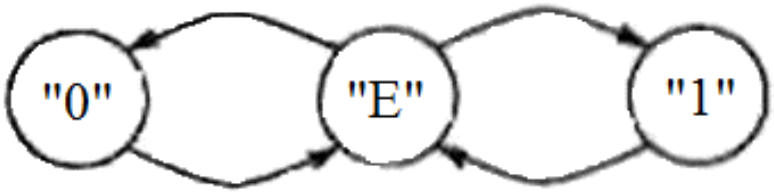



# 2-phase bundled data protocol

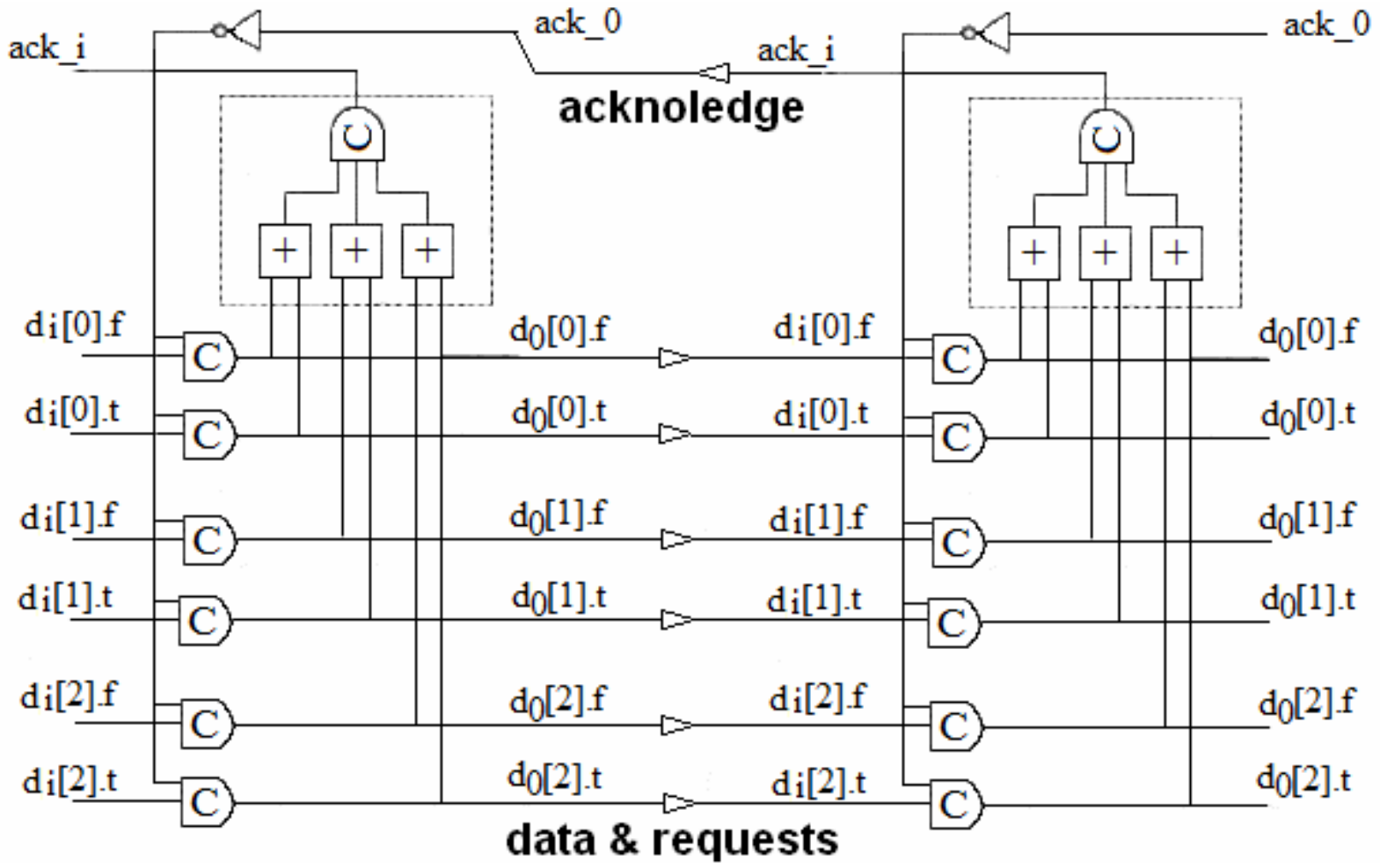


# Dual-rail signals

| | d.t | d.f |
|---|---|---|
| Empty state "E" | 0 | 0 |
| Logic "0" | 0 | 1 |
| Logic "1" | 1 | 0 |
| Forbidden state | 1 | 1 |



# Dual-rail FIFO pipeline



# Complete truth table for dual-rail AND

| a.f a.t | b.f b.t | y.f y.t |
|---|---|---|
| 00 | 00 | 00 |
| 00 | 01 | 00 |
| 00 | 10 | 00 |
| 00 | 11 | - |
| 01 | 00 | 00 |
| 01 | 01 | 01 |
| 01 | 10 | 10 |
| 01 | 11 | - |
| 10 | 00 | 00 |
| 10 | 01 | 10 |
| 10 | 10 | 10 |
| 10 | 11 | - |
| 11 | 00 | - |
| 11 | 01 | - |
| 11 | 10 | - |
| 11 | 11 | - |

# Complete truth table for dual-rail AND

| a.f a.t | b.f b.t | y.f y.t |
|---|---|---|
| 00 | 00 | 00 |
| 00 | 01 | 00 |
| 00 | 10 | 00 |
| 00 | **11** | - |
| 01 | 00 | 00 |
| 01 | 01 | 01 |
| 01 | 10 | 10 |
| 01 | **11** | - |
| 10 | 00 | 00 |
| 10 | 01 | 10 |
| 10 | 10 | 10 |
| 10 | **11** | - |
| **11** | 00 | - |
| **11** | 01 | - |
| **11** | 10 | - |
| **11** | **11** | - |

# Truth table for dual-rail AND

| a.f a.t | b.f b.t | y.f y.t |
|---|---|---|
| 00 | 00 | 00 |
| 00 | 01 | 00 |
| 00 | 10 | 00 |
| 01 | 00 | 00 |
| 01 | 01 | 01 |
| 01 | 10 | 10 |
| 10 | 00 | 00 |
| 10 | 01 | 10 |
| 10 | 10 | 10 |

# Truth table for dual-rail AND

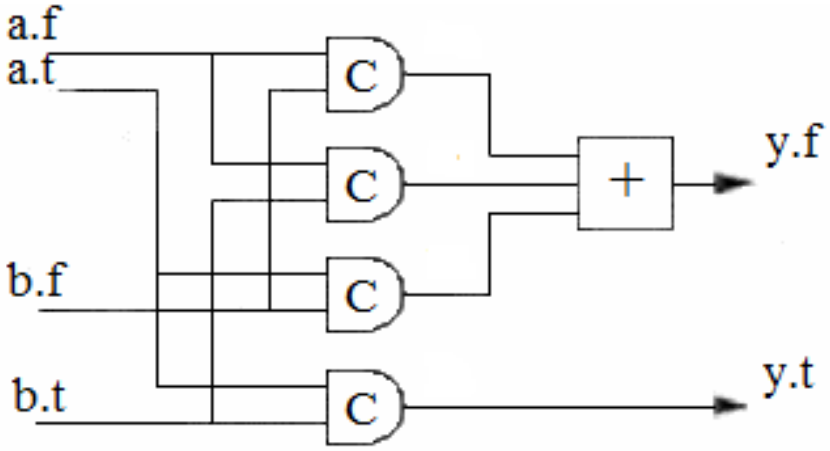
| a.f a.t | b.f b.t | y.f y.t |
|---|---|---|
| 00 | 00 | 00 |
| 00 | 01 | 00 |
| 00 | 10 | 00 |
| 01 | 00 | 00 |
| **01** | **01** | **01** |
| **01** | **10** | **10** |
| 10 | 00 | 00 |
| **10** | **01** | **10** |
| **10** | **10** | **10** |

# Construction of dual-rail AND

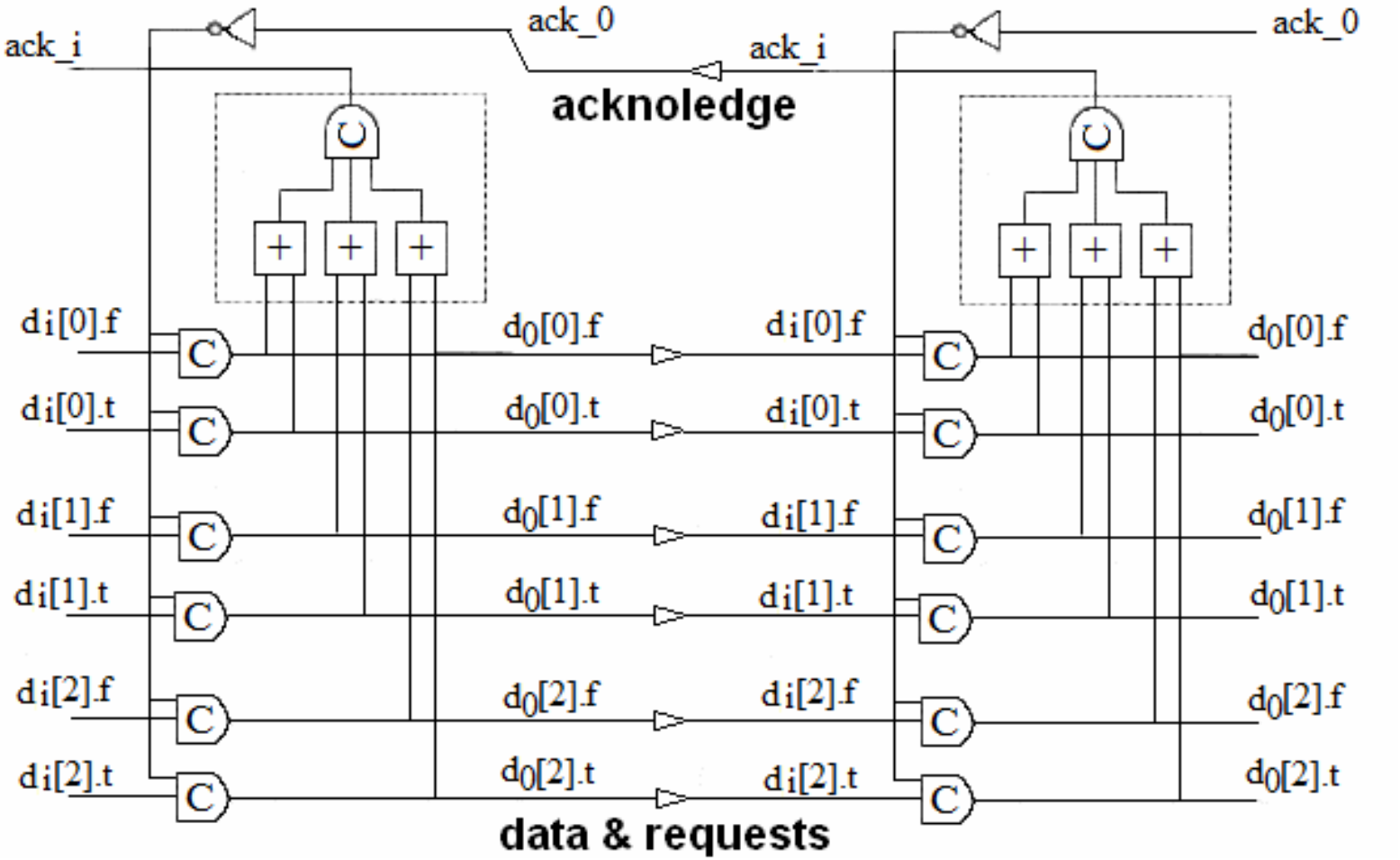
| a.f<br>a.t | b.f<br>b.t | C1 | C2 | C3 | C4 | y.f<br>y.t |
|---|---|---|---|---|---|---|
| 00 | 00 | 0 | 0 | 0 | 0 | 00 |
| 00 | 01 | 0 | 0 | 0 | 0 | 00 |
| 00 | 10 | 0 | 0 | 0 | 0 | 00 |
| 01 | 00 | 0 | 0 | 0 | 0 | 00 |
| **01** | **01** | **0** | **0** | **0** | **1** | **01** |
| **01** | **10** | **0** | **0** | **1** | **0** | **10** |
| 10 | 00 | 0 | 0 | 0 | 0 | 00 |
| **10** | **01** | **0** | **1** | **0** | **0** | **10** |
| **10** | **10** | **1** | **0** | **0** | **0** | **10** |

$$y.f = a.t \,\&\, b.t \mid a.t \,\&\, b.f \mid a.f \,\&\, b.t$$

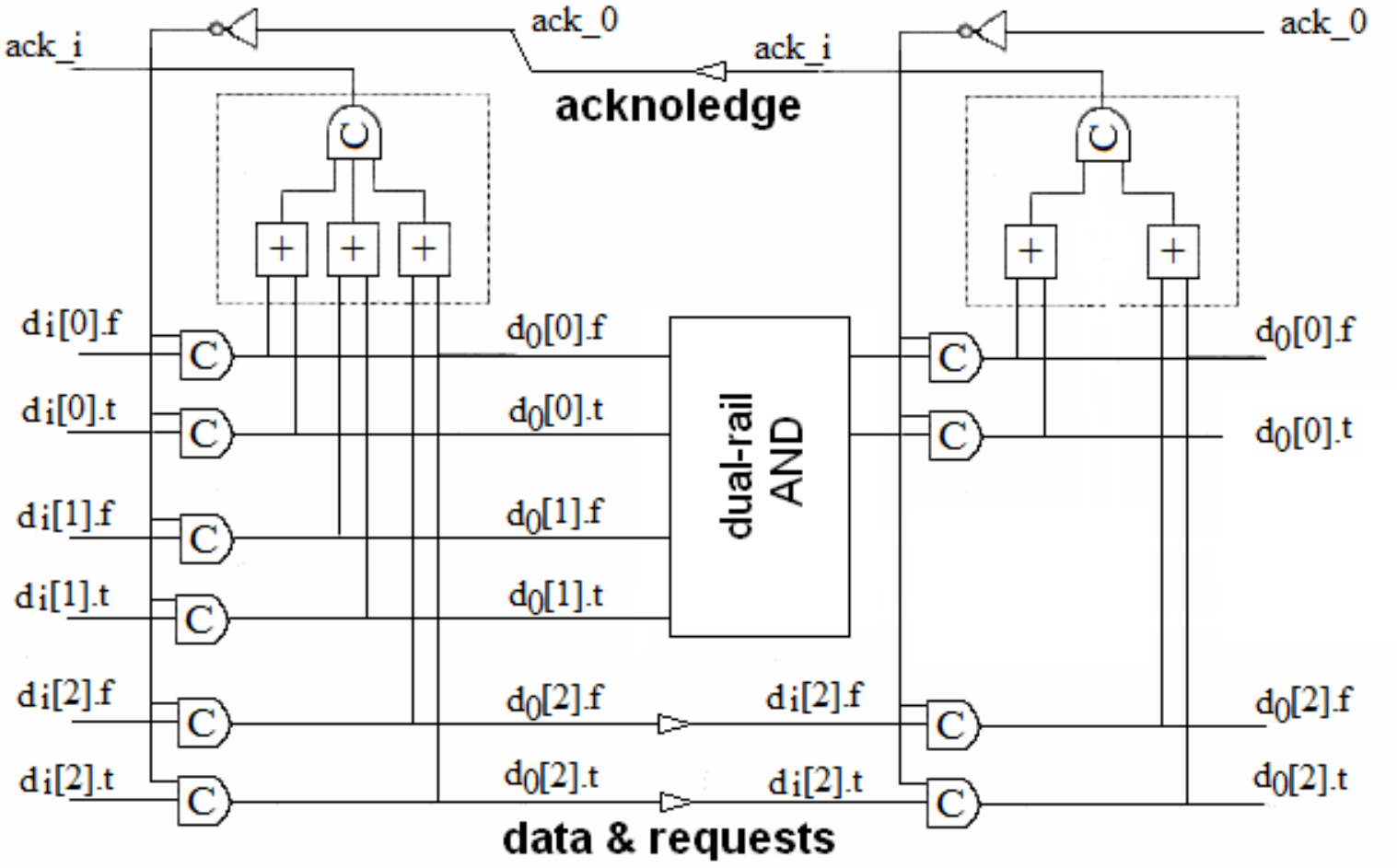
$$y.t = a.f \,\&\, b.f$$



# Dual-rail FIFO circuit



# Dual-rail AND circuit



# Self-timed protocols types

- Dual-rail or Bundled-data.
- 2-phase or 4-phase.
- Push channel or pull channel.

# Self-timed circuit advantages

- **No clock distribution and clock skew problems**,
  there is no global signal that needs to be distributed with minimal phase skew across the circuit
- **Less power consumption**
  due to fine-grain clock gating and zero standby power consumption.
- **Native operating speed**
  operating speed is determined by actual local latencies rather than global worst-case latency.
- **Small emission of electro-magnetic noise**
  the local clocks tend to tick at random points in time.
- **Robustness towards variations in supply voltage, temperature, and fabrication process parameters.**
  timing is based on matched delays (and can even be insensitive to circuit and wire delays).

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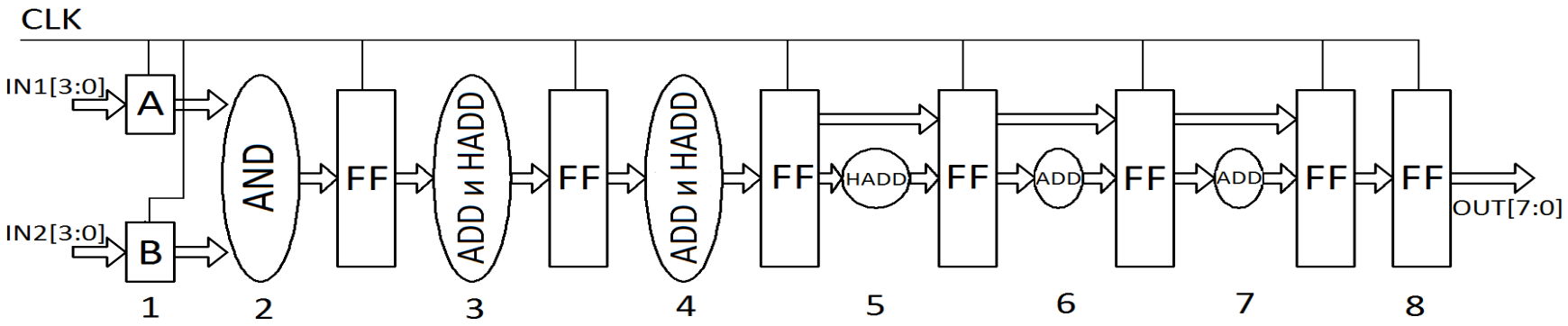
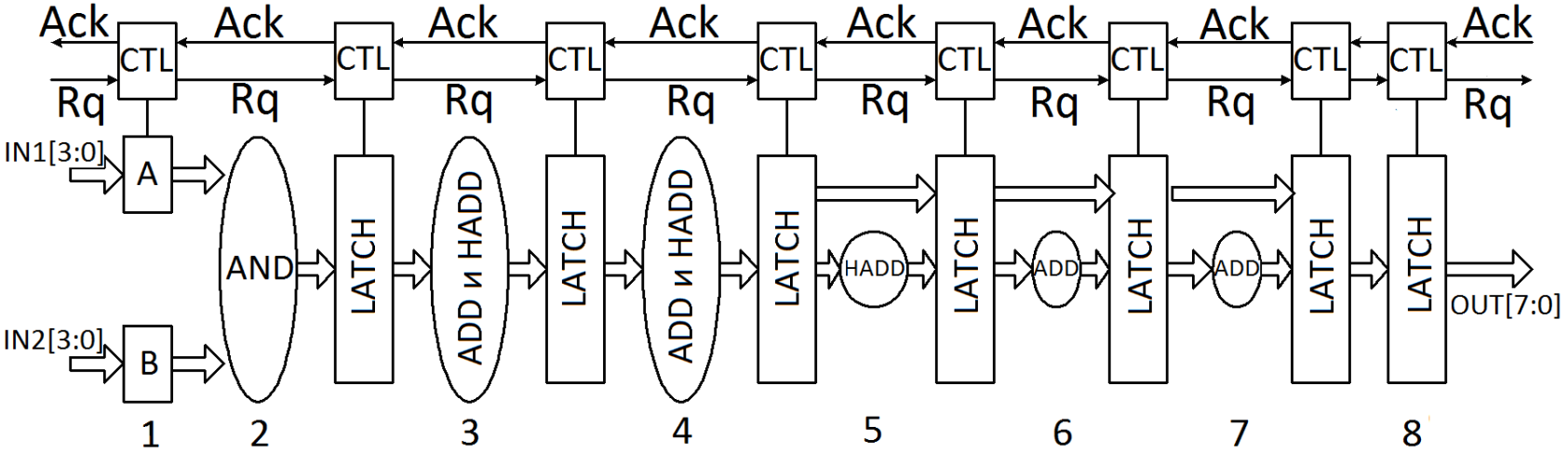
# Parallel multiplier implementations




Synchronous design

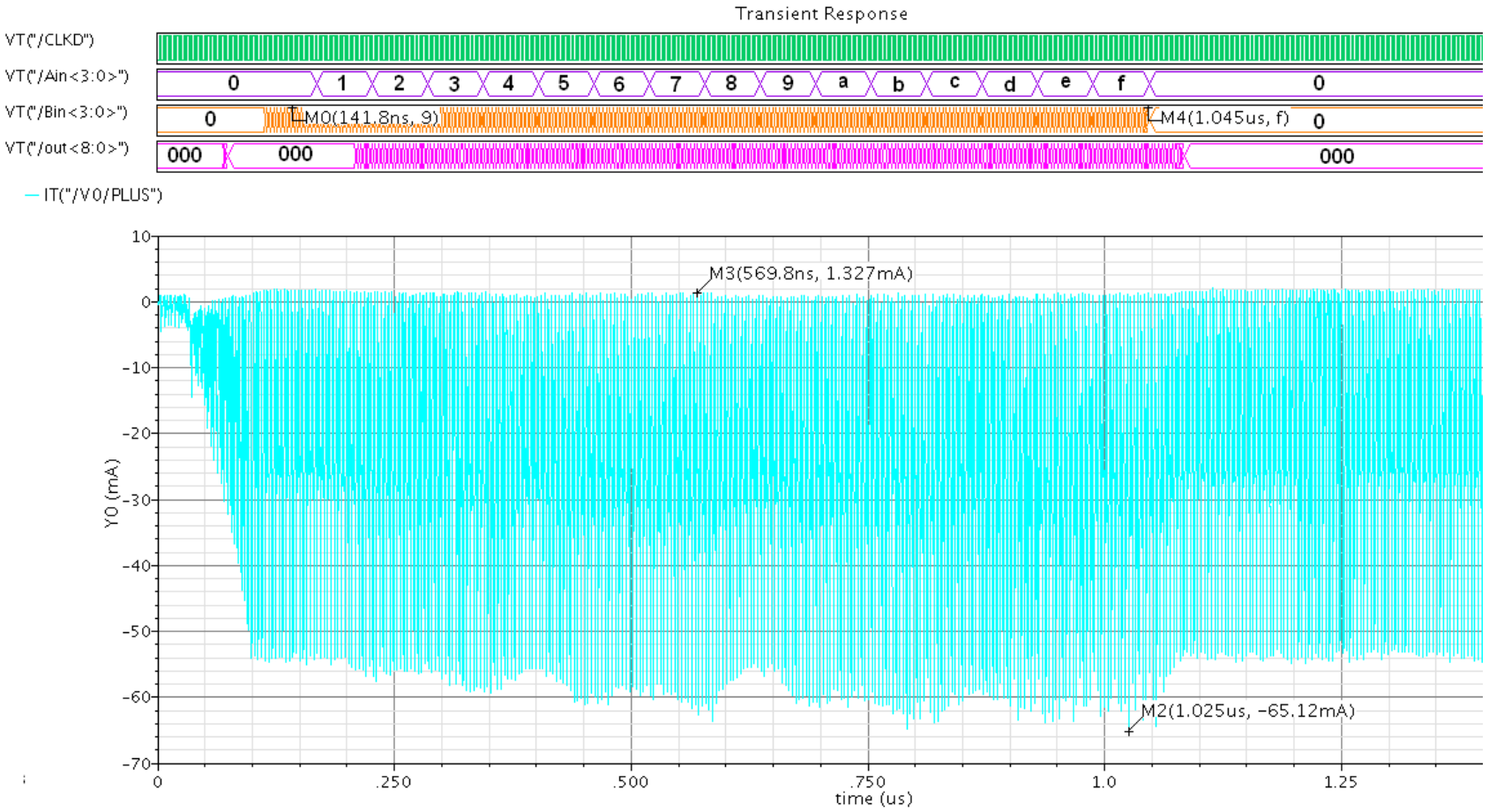



Asynchronous design

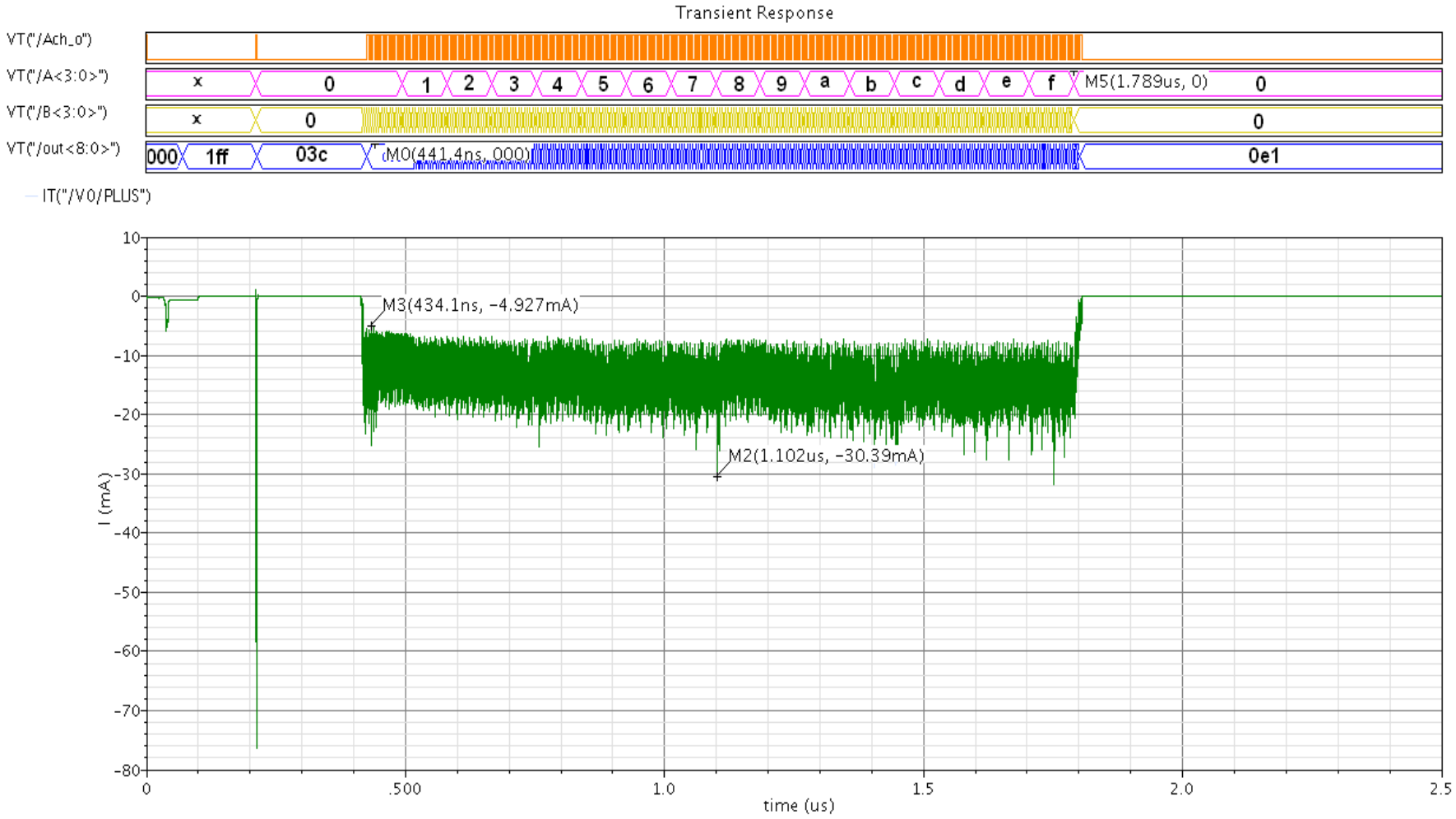
# Compare designs table

| | Synchronous design | | Asynchronous design | |
|---|---|---|---|---|
| | single | stream | single | stream |
| Period (equivalent for asynchronous) (ns) | 3,66 | 3,66 | 2,8 | 3,4 |
| Max temp (C) | 66 | | >200 | |
| Avr. current (mA) | 12,02 | 20 | 0,29 | 14 |
| Max current (mA) | 18,9 | 65.12 | 5,95 | 30.39 |

# Synchronous circuit current consumption diagram



# Self-timed circuit current consumption diagram



Thank You!